Michael J. Hall

Curriculum Vitae

St. Louis, Missouri – USA
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Education

May 2015 **Washington University in St. Louis**, *Doctor of Philosophy in Computer Engineering*, St. Louis, MO
Dissertation: Utilizing Magnetic Tunnel Junction Devices in Digital Systems
Advisor: Dr. Roger Chamberlain
Co-advisor: Dr. Viktor Gruev
Grade Point Average: 4.0/4.0

December 2007 **Southern Illinois University Edwardsville**, *Master of Science in Electrical Engineering*, Edwardsville, IL
Thesis: Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation
Advisor: Dr. George Engel
Grade Point Average: 4.0/4.0

May 2006 **Southern Illinois University Edwardsville**, *Bachelor of Science in Computer Engineering*, Edwardsville, IL
Minor: Computer Science
Senior Design Project: IEEE 2006 Robot Competition
Grade Point Average: 4.0/4.0

June 2002 **Cisco Networking Academy**, *Cisco Certified Network Associate (CCNA), expired*
Certification valid 2002–2005

Academic Appointments

Fall 2024 – Present **Washington University in St. Louis**, *Lecturer*, St. Louis, MO
- Departments of Computer Science & Engineering, and Electrical & Systems Engineering
- Teach and manage undergraduate and graduate-level courses.
- Develop course materials and assignments.
- Supervise teaching assistants, proctor exams, grade student work, and hold office hours.
- Advise students and write letters of recommendation.

Spring 2020 – Spring 2024 **Washington University in St. Louis**, *Adjunct Instructor*, St. Louis, MO
- Department of Computer Science & Engineering
- Created new course assignments and instructional materials.
- Conducted recitation sessions, managed TAs, proctored exams, graded coursework, offered office hours, and wrote letters of recommendation for students.

Work Experience

October 2023 – Present **Hailey Hall Art, LLC**, *Vice-President with Technical Lead*, St. Louis, MO
- Edited and published a children's book as part of a family-owned LLC supporting Hailey Hall's creative works.
- Manage business operations, including the website, marketing, and financial records.

December 2021 – August 2024 **OpenVault**, *Software Engineer*, Jersey City, NJ
- Implemented Profile Management Application (PMA) algorithm in Python, including K-Means clustering, segmentation, scoring, and database integration.
- Built central metrics collector system for DevOps monitoring (Prometheus, Grafana, Docker Compose).
- Led backend engineering, database optimization, and DevOps deployment.
- Developed machine learning models, dashboards, and data pipelines from whitepaper to production.

March 2015 – December 2021 **VelociData**, *Hardware Engineer*, St. Louis, MO
- Developed high-performance algorithms and systems for fast protocol parsing, output generation, parallel processing, and IPDR/NetFlow collection.
- Measured system performance, identified bottlenecks, and optimized throughput.
- Analyzed data using statistics and generated visualizations.

April 2014 – December 2019 **Independent Collaboration**, *Technical Editor*, St. Louis, MO
- Book: *The Art of Computer Systems Performance Analysis: Techniques for Experimental Design, Measurement, Simulation, and Modeling*
- Collaborated with Dr. Raj Jain, author of the book, as technical editor.
- Reviewed chapters for technical accuracy and clarity.
- Verified examples and equations through derivation and Monte Carlo methods.

January 2008 – Spring 2015 **Washington University in St. Louis**, *Graduate Research Assistant*, St. Louis, MO
- Designed digital logic circuits using magnetic devices.
- Developed context-switched hardware blocks for reconfigurable computing.

May 2013 – December 2013 **VelociData**, *Hardware Engineering Intern*, St. Louis, MO
- Designed and implemented an SHA cryptographic hash function in SystemVerilog using C-slow techniques.
- Verified correctness with randomized tests in C++.

June 2012 – August 2012 **MIT Lincoln Laboratory**, *Summer Intern*, Lexington, MA
- Continued design of a high-speed digital implementation of a frame synchronization algorithm in VHDL.

June 2011 – August 2011 **MIT Lincoln Laboratory**, *Summer Intern*, Lexington, MA
- Designed a high-speed digital implementation of a frame synchronization algorithm in VHDL.

May 2009 – August 2009 **DRS Sustainment Systems**, *Electrical Engineering Intern*, St. Louis, MO
- Designed, analyzed, and simulated a servo amplifier card.

May 2006 – December 2007 **Southern Illinois University Edwardsville**, *Research Assistant*, Edwardsville, IL
- Designed a new pulse-shape discrimination (PSD) chip.
- Revised and fabricated the heavy-ion nuclear physics 16-channel (HINP16C) chip.
- Maintained lab computers and Cadence design tools.

May 2004 – January 2008 **Alton Steel, Inc.**, *Computer Programmer*, Alton, IL
- Developed Visual Basic frontend applications, backend SQL scripts, and Crystal Reports.
- Collaborated with users to determine requirements and deliver solutions.

Teaching

2020 – Present **Washington University in St. Louis**, *Lecturer*, St. Louis, MO
- CSE 560M Computer Systems Architecture I (Fall 2021, Fall 2022, Fall 2024)
- CSE 462M Computer Systems Design (Spring 2025)
- CSE 362M Computer Architecture (Fall 2024)
- CSE 260M Introduction to Digital Logic and Computer Design (Spring 2025)
- CSE 132 Intro to Computer Engineering (Spring 2020, Fall 2020, Fall 2023)
- ESE 498 Electrical Engineering Capstone Design Projects (Fall 2024)

2019 **Self-Employed**, *Statistics Tutor for a Maryville University Student*, St. Louis, MO
- SOSC 341 Understanding Statistical Inference (Summer 2019)

2011 – 2013 **Washington University in St. Louis**, *Teaching Assistant*, St. Louis, MO
- CSE 567M Computer Systems Analysis (Spring 2011, Spring 2013)

Graduate Committee Memberships

1. Binglin (Kevin) Ji — *Accelerating GNN Inference On Multi-core Systems*
   Master's Thesis, M.S. in Electrical Engineering, Washington University in St. Louis
   Defense Date: August 11, 2025

2. Carmen Bland Jr — *Racial Bias in Pulse Oximetry*
   Master's Project, M.S. in Computer Engineering, Washington University in St. Louis
   Defense Date: August 11, 2025

3. Qinzhou (Nick) Song — *Generalization of ADAPT HLS Computational Pipeline*
   Master's Thesis, M.S. in Computer Science, Washington University in St. Louis
   Defense Date: April 30, 2025

4. Longhao Huang — *New Signal Identification Algorithms for Enhanced Gamma-Ray Burst Detection in the Advanced Particle-Astrophysics Telescope*
   Master's Thesis, M.S. in Electrical Engineering, Washington University in St. Louis
   Defense Date: April 24, 2025

5. Varad Deouskar — *Adapt Dashboard and Visualizer*
   Master's Project, M.S. in Computer Science, Washington University in St. Louis
   Defense Date: December 16, 2024

6. Zaid Ahmed — *Compressing Context for Large Language Models*
   Master's Project, M.S. in Computer Engineering, Washington University in St. Louis
   Defense Date: December 13, 2024

Publications

Peer-Reviewed

1. Bill Siever, **Michael Hall**, Jim Feher, and Roger Chamberlain, "Teaching Digital Logic and Computer Architecture Using Open Source Tools," in *Proc. of 22nd ACM International Conference on Computing Frontiers Workshops and Special Sessions*, May 2025, pp. 53–56. doi: 10.1145/3706594.3726971. Presented at 3rd Open Source Hardware Workshop (OSHW), Cagliari, Sardinia, Italy.

2. Bill Siever, **Michael Hall**, Jim Feher, and Roger Chamberlain, "Digital logic, computer architecture, and dev containers: Supporting schools from little to large," in *Proceedings of the 56th ACM Technical Symposium on Computer Science Education V.2*, Feb. 2025, pp. 1737–1737. *(Published abstract and conference demo)*. doi: 10.1145/3641555.3705024.

3. **Michael J. Hall**, Neil E. Olson, and Roger D. Chamberlain, "Utilizing Virtualized Hardware Logic Computations to Benefit Multi-User Performance," *Electronics* 2021, 10(6), 665, Mar 2021. doi: 10.3390/electronics10060665

4. **Michael J. Hall**, Neil Olson, and Roger Chamberlain, "Data from Virtualized Hardware Logic Computations" (2021). Digital Research Materials (Data & Supplemental files). 60. `https://openscholarship.wustl.edu/data/60`. doi: 10.7936/46pb-xw44

5. **Michael J. Hall**, Viktor Gruev, and Roger D. Chamberlain, "Characterization of a binary output resistance-to-voltage read circuit for sensing magnetic tunnel junctions," *IEEE Sensors Journal*, vol. 18, no. 3, pp. 1023–1031, Feb 2018. doi: 10.1109/jsen.2017.2780112

6. **Michael J. Hall**, and Roger D. Chamberlain. "Using M/G/1 queueing models with vacations to analyze virtualized logic computations," in *2015 33rd IEEE Int'l Conf. on Computer Design (ICCD)*, Oct. 2015, pp. 78–85. doi: 10.1109/iccd.2015.7357087

7. **Michael J. Hall**, Roger D. Chamberlain. "Performance modeling of virtualized custom logic computations," in *Proc. of the 25th IEEE Int'l Conf. on Application-specific Systems Architectures and Processors (ASAP)*, Jun. 2014. doi: 10.1109/asap.2014.6868635

8. **Michael J. Hall**, Roger D. Chamberlain. "Performance modeling of virtualized custom logic computations," in *Proc. of the 24th ACM Int'l Great Lakes Symposium on VLSI*, 2014. doi: 10.1145/2591513.2591570

9. **Michael J. Hall**, Viktor Gruev, Roger D. Chamberlain. "Performance of a resistance-to-voltage read circuit for sensing magnetic tunnel junctions," *Circuits and Syst. (MWSCAS), 2012 IEEE 55th Int. Midwest Symp.*, August 2012. doi: 10.1109/mwscas.2012.6292101

10. **Michael J. Hall**, Viktor Gruev, Roger D. Chamberlain. "Noise analysis of a current-mode read circuit for sensing magnetic tunnel junction resistance," *Circuits and Syst. (ISCAS), 2011 IEEE*, May 2011. doi: 10.1109/iscas.2011.5937938

11. Linda M. Engelbrecht, Albrecht Jander, Pallavi Dhagat, **Michael J. Hall**. "A toggle MRAM bit modeled in Verilog-A," *Solid-State Electronics*, vol. 54, no. 10, pp. 1135–1142, Oct. 2010. Selected Papers from ISDRS 2009. doi: 10.1016/j.sse.2010.05.038

12. Roger Chamberlain, Mark Franklin, Eric Tyson, James Buckley, Jeremy Buhler, Greg Galloway, Saurabh Gayen, **Michael Hall**, Berkley Shands, and Naveen Singla. "Auto-Pipe: Streaming applications on architecturally diverse systems," *Computer*, vol. 43, pp. 42–49, 2010. doi: 10.1109/mc.2010.62

13. George L. Engel, **Michael J. Hall**, Justin M. Proctor, Jon M. Elson, Lee G. Sobotka, Rebecca S. Shane, Robert J. Charity. "Design and performance of a multi-channel, multi-sampling, PSDenabling integrated circuit," *Nuclear Instruments and Meth. A*, vol. 612, no. 1, pp. 161–170, 2009. doi: 10.1016/j.nima.2009.10.058

14. Raphael Njuguna, **Michael Hall**, and Vicktor Gruev. "Low power CMOS image sensor with programmable spatial filtering," in *IEEE Sensors 2009*, 2009, pp. 189–192. doi: 10.1109/icsens.2009.5398196

15. **Michael Hall**, Albrecht Jander, Roger D. Chamberlain, and Pallavi Dhagat, "Globally Clocked Magnetic Logic Circuits," in Digest of International Magnetics Conference (Intermag), May 2009.

16. Naveen Singla, **Michael Hall**, Berkley Shands, and Roger D. Chamberlain. "Financial Monte Carlo simulation on architecturally diverse systems," in *Workshop on High Perf. Comput. Finance, 2008*. WHPCF 2008., 2008, pp. 1–7. doi: 10.1109/whpcf.2008.4745401

Dissertation & Thesis

1. **Michael J. Hall**. "Utilizing Magnetic Tunnel Junction Devices in Digital Systems," Ph.D. dissertation, Dept. of Computer Science and Engineering, Washington University in St. Louis, May 2015. doi: 10.7936/K7PN93RH

2. **Michael J. Hall**. "Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation," M.S. Thesis, Dept. of Elect. Eng., SIUE, Dec 2007. doi: 10.13140/RG.2.2.36309.54240

Presentations

Conference Presentations

1. **Michael Hall**, "Using M/G/1 Queueing Models with Vacations to Analyze Virtualized Logic Computations," Presented at the 33rd IEEE International Conference on Computer Design, New York, NY, USA, October 19, 2015. [slides]
2. **Michael Hall**, "Performance of a Resistance-To-Voltage Read Circuit for Sensing Magnetic Tunnel Junctions," Presented at the 55th IEEE International Midwest Symposium on Circuits and Systems, Boise, Idaho, USA, August 7, 2012. [slides]
3. **Michael Hall**, "Noise Analysis of a Current-Mode Read Circuit for Sensing Magnetic Tunnel Junction Resistance," Presented at IEEE International Symposium on Circuits and Systems (ISCAS), Rio de Janeiro, Brazil, May 17, 2011. [slides]
4. **Michael Hall**, "Globally Clocked Magnetic Logic Circuits," Presented at IEEE International Magnetic Conference, Sacramento, CA, USA, May 5, 2009. [slides]
5. **Michael Hall**, "Development of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Important," Presented in the Central States Universities Incorporated Research Conference, Argonne National Laboratory, Lemont, IL, USA, November 2, 2007. [slides]

Academic Presentations

1. **Michael Hall**, "Utilizing Magnetic Tunnel Junctions in Digital Systems," Dissertation Defense, Presented in the Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, April 10, 2015. [slides]
2. **Michael Hall**, "Evaluating MTJ Benefits and Utilizing Context-Switched Hardware for Designing Magnetologic Circuits," Dissertation Proposal Defense, Presented in the Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, May 23, 2013. [slides]
3. **Michael Hall**, "Magnetic Random Access Memory (MRAM)," Oral Qualifications, Presented in the Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, November 11, 2009. [slides]
4. **Michael Hall**, "Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation," Master's Thesis Defense, Department of Electrical and Computer Engineering, Southern Illinois University Edwardsville, Edwardsville, IL, USA, December 13, 2007. [slides]
5. **Michael Hall**, "Development of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Important," Presented at SIUE Graduate Student Research Symposium, Southern Illinois University Edwardsville, Edwardsville, IL, USA, April 3, 2007. [slides]

6. **Michael Hall**, Eddie Inlow, and Jeff Croxell, "IEEE 2006 Robot Competition," Presented as the senior design project for ECE 405 at Southern Illinois University Edwardsville, in completion of the B.S. in Computer Engineering, May 2006.

Posters

1. **Michael Hall**, Roger D. Chamberlain, "Virtualization of Deeply Pipelined Magnetologic," Poster presented at the 2017 IEEE International Conference on Rebooting Computing (ICRC), Washington, DC, USA, November 9, 2017. [poster]
2. **Michael J. Hall**, Roger D. Chamberlain, "Performance Modeling of Virtualized Custom Logic Computations," Poster presented at the 2014 IEEE 25th International Conference on Application-Specific Systems, Architectures and Processors, Zurich, Switzerland, June 18 – 20, 2014. [poster]
3. **Michael J. Hall**, Roger D. Chamberlain, "Performance Modeling of Virtualized Custom Logic Computations," Poster presented at the 24th International Great Lakes Symposium on VLSI, May 21 – 23, 2014. [poster]

Creative Works

1. Hailey K. Hall, *An Aunt's Animal Alphabet: From A to Z, Come Rhyme with Me - A Whimsical Breeze Through the ABCs!*, **Michael J. Hall**, Ed., Hailey Kathleen Hall: St. Louis, 2023. ISBN: 979-8987233801 (hardcover), 979-8987233825 (paperback). Available: Author's Website, Amazon, Inside Preview

Selected Engineering Projects

2021 – 2024 **Profile Management Application (PMA) Development**, *OpenVault*

- Implemented PMA algorithms in Python, based on publicly available whitepapers.
- Developed features including K-Means clustering, profile segmentation and assignment, statistical analysis, and scoring functions.
- Integrated with a database to transform data into the required format and generate reports.

2023 **Centralized DevOps Monitoring System**, *OpenVault*

- Built a centralized metrics collection system for product monitoring.
- Set up an Ubuntu host system with Linux Containers (LXC) to run services including Prometheus, Grafana, Nginx, Postfix, Prometheus exporters, and SSH tunnels.
- Used Docker Compose for simplified service deployment and upgrades.

2011 – 2015 **Virtualized Hardware Logic Circuits**, *Washington University in St. Louis*, CSE Department, PhD Research

- Developed a hardware architecture enabling context switching within pipelined circuits to efficiently handle computations with long feedback paths.
- Designed and implemented example applications including a synthetic cosine function, AES encryption, and SHA-2 hashing.
- Evaluated performance through simulation and FPGA implementation, demonstrating improved throughput and resource utilization.

2011 – 2015 **Magnetic Tunnel Junction (MTJ) Read Circuit and Test Chip Development**, *Washington University in St. Louis*, CSE Department, PhD Research

- Designed an MTJ read circuit to evaluate the feasibility of magnetic global clocking.
- Fabricated a prototype test chip using a 3-metal, 2-poly (3M2P) 0.5 μm CMOS process.
- Developed a custom PCB, interfacing it with an Opal Kelly FPGA board.
- Programmed custom FPGA firmware and supporting Python software.
- Conducted experimental evaluation of the MTJ read circuit using the prototype system.

2008 – 2010 **FPGA Data Acquisition Controller for Radiation Detection**, *Washington University in St. Louis*, Radiochemistry Group

- Developed an FPGA controller for interfacing with and acquiring data from experimental channels used in ionizing radiation detection.

2009 **Optical Communication Prototype with Image Sensor and LED**, *Washington University in St. Louis*, CSE Department, Graduate Course Project

- Designed a prototype PCB for an image sensor and LED system enabling optical communication over distance.

2006 – 2007 **Pulse-Shape Discrimination (PSD) IC Design and Simulation**, *Southern Illinois University Edwardsville*, VLSI Design Research Laboratory, Joint Research with Washington University in St. Louis (Radiochemistry)

- Designed, modeled, and simulated a pulse-shape discrimination (PSD) chip for nuclear physics experiments under the supervision of Dr. George Engel.

Technical Skills

Hardware Digital design, IC design and layout, FPGA synthesis, PCB design and layout, microcontrollers, digital signal processing (DSP), soldering, computer networking

Languages C/C++, Python, Visual C++, Visual Basic .NET, Verilog, SystemVerilog, VHDL, SQL, Bash

Software Cadence IC design tools, PSpice, Xilinx Vivado, Intel Quartus, ModelSim, Synplicity; Mathcad, Mathematica, MATLAB, Python scientific libraries (NumPy, SciPy, Matplotlib, pandas), Jupyter Notebooks; Nginx, Django; PostgreSQL, SQL Server 2000; Grafana, Prometheus; JetBrains IDEs (PyCharm, CLion, DataGrip, IntelliJ); Git, Subversion; Windows (10, 7, XP, 2003 Server), FreeBSD, Linux; ZFS, Linux Containers (LXC), Docker, Docker Compose, Terraform; Adobe InDesign, GIMP, CorelDRAW, WordPress

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