MICHAEL J. HALL

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EDUCATION

Washington University in St. Louis (WUSTL) St. Louis, MO
Degree: **Doctor of Philosophy in Computer Engineering** May 2015
Thesis topic: Utilizing Magnetic Tunnel Junction devices in digital systems
Advisor: Dr. Roger Chamberlain
Co-advisor: Dr. Viktor Gruev
Grade Point Average: 4.0 / 4.0

Southern Illinois University Edwardsville (SIUE) Edwardsville, IL
Degree: **Master of Science in Electrical Engineering** December 2007
M.S. thesis topic: Integrated circuit for the detection of ionizing radiation
Advisor: Dr. George Engel
Grade Point Average: 4.0 / 4.0

Southern Illinois University Edwardsville (SIUE) Edwardsville, IL
Degree: **Bachelor of Science in Computer Engineering** May 2006
Minors: Mathematics
Computer Science
Grade Point Average: 4.0 / 4.0

Cisco Network Academy
Certification: Cisco Certified Network Associate (expired) June 2002

ENGINEERING EXPERIENCE

PMA Algorithm Design OpenVault 2021 – 2024
Activities:
- Implemented whitepapers on Profile Management Application (PMA) algorithm in Python.
- Features include K-Means machine learning, profile segmentation algorithm, profile assignments, statistics calculations, and scoring function.
- Interact with database, transform data into the required form, and report results.

DevOps framework OpenVault 2022 – 2023
Activities:
- Built a central metrics collector system for DevOps monitoring of products.
- Setup Ubuntu host system with Linux Containers (LXC) for running services. Services include Prometheus, Grafana, Nginx, Postfix, Prometheus exporters, and SSH tunnels.
- Deploy services via Docker compose for easy deployment and upgrades.

Test Chip Design Washington University 2011 – 2015
Activities:
- Designed a magnetic tunnel junction (MTJ) read circuit for evaluating the feasibility of magnetic global clocking.
- Designed and fabricated a prototype test chip in a 3 metal 2 poly (3M2P) 0.5 μm process.
- Designed and fabricated a PCB board and interfaced it with an Opal Kelly FPGA board.
- Developed custom FPGA firmware and custom Python software.
- Evaluated MTJ read circuit experimentally with prototype setup.

FPGA Controller Washington University Radiochemistry group 2008 – 2010
Activities:
- Developed an FPGA controller for interfacing with and acquiring data from channels in an experimental system used for the detection of ionizing radiation.

PCB Board Design Optical communications using image sensor May 2009
Activities: ▪ Designed a PCB prototype board for an image sensor and a light-emitting diode (LED) that communicates optically over a distance.

IC Design Washington University Radiochemistry group 2006 – 2007
Activities: ▪ Designed, analytical modeled, and simulated a pulse-shape discrimination (PSD) chip for use in nuclear physics experiments.

TEACHING EXPERIENCE

Washington University in St. Louis (WUSTL) St. Louis, MO

Lecturer	CSE 560M Computer Systems Architecture I	Fall 2024
	CSE 362M Computer Architecture	Fall 2024
	ESE 498 Electrical Engineering Capstone Design Projects	Fall 2024
Adjunct Instructor	CSE 132 Intro to Computer Engineering	Fall 2023
		Spring 2020, Fall 2020
	CSE 560M Computer Systems Architecture I	Fall 2021, Fall 2022
Teaching Assistant	CSE 567M Computer Systems Analysis	Spring 2011, Spring 2013

GRADUATE DEFENSE COMMITTEES

1. Varad Deouskar, *Adapt Dashboard and Visualizer*, Master's Project Defense, Master of Science in Computer Science, Washington University in St. Louis, December 16, 2024.
2. Zaid Ahmed, *Compressing Context for Large Language Models*, Master's Project Defense, Master of Science in Computer Engineering, Washington University in St. Louis, December 13, 2024.

WORK EXPERIENCE

Washington University in St. Louis September 2024 – Present St. Louis, MO
Position: Lecturer
Departments: Computer Science & Engineering
Electrical & Systems Engineering
Responsibilities: ▪ Teach and manage courses, lecture on topics, manage TAs, proctor exams, grade student work, and hold office hours
▪ Develop course materials
▪ Advise students and write recommendation letters

Washington University in St. Louis January 2020 – August 2024 St. Louis, MO
Position: Adjunct Instructor
Courses: CSE 132 and CSE 560M
Responsibilities: ▪ Teach and manage courses, lecture on topics, hold recitation reviews, manage TAs, proctor exams, grade student work, and hold office hours
▪ Develop new course assignments
▪ Write recommendations for students

OpenVault December 2021 – August 2024 Jersey City, NJ
Position: Software Engineer
Responsibilities: ▪ Built the whole application DevOps framework
▪ Built and maintained the core machine learning algorithm for network optimization product
▪ Highly engaged in design and architecture at the highest level
▪ Team leader mentoring of advanced machine learning
▪ Designed and optimized database infrastructure
▪ Backend software engineering
▪ Data science with machine learning, dashboards, databases, and statistics
▪ Deep topic research
▪ Going from white paper to working product

VelociData March 2015 – December 2021 St. Louis, MO

Position: Hardware Engineer

Responsibilities:
- Develop high-performance algorithms, components, and systems including fast protocol parsing, fast output generation, parallel processing, network packet processing, and IPDR and Netflow collectors
- Measure system performance, identify bottlenecks, and optimize
- Analyze data with statistics and generate visualizations

Hailey Hall Art October 2023 – Present St. Louis, MO

Position: Vice-President with Technical Lead

Responsibilities:
- Edit and publish *An Aunt's Animal Alphabet* book by Hailey Hall
- Do market research, optimize book metadata, and get editorial reviews
- Host and maintain author website
- Setup POS system for sales, and manage financials

Technical Editor April 2014 – Present St. Louis, MO

Book: The Art of Computer Systems Performance Analysis: Techniques for Experimental Design, Measurement, Simulation, and Modeling

Responsibilities:
- Review each chapter for technical correctness
- Solve every example and problem, and verify equations via derivation and/or Monte Carlo techniques
- Clarify text and revise as necessary for consistency

Statistics Tutor June 2019 – July 2019 St. Louis, MO

Course: SOSC 341, Understanding Statistical Inference

Responsibilities:
- Explained statistics concepts, worked examples and problems, and prepared for quizzes and exams

Washington University in St. Louis January 2008 – Spring 2015 St. Louis, MO

Position: Graduate Research Assistant

Research Areas:
- Digital logic design using magnetic devices
- Context-switched hardware blocks

VelociData May 2013 – December 2013 St. Louis, MO

Position: Hardware Engineering Intern

Responsibilities:
- Designed and implemented an SHA cryptographic hash function in SystemVerilog using C-slow techniques
- Verified correctness with randomized tests written in C++

MIT Lincoln Laboratory June 2012 – August 2012 Lexington, MA
June 2011 – August 2011

Position: Summer Intern

Responsibilities:
- Designed a high-speed digital implementation of a frame synchronization algorithm in VHDL

DRS Sustainment Systems May 2009 – August 2009 St. Louis, MO

Position: Electrical Engineering Intern

Responsibilities:
- Designed, analyzed, and simulated a servo amplifier card

Southern Illinois University Edwardsville May 2006 – December 2007 Edwardsville, IL

Position: Research Assistant

Responsibilities:
- Designed new pulse-shape discrimination (PSD) chip
- Revised and fabricated the heavy-ion nuclear physics, 16 channel (HINP16C) chip
- Maintained lab computers and Cadence design tools

Alton Steel, Inc. May 2004 – January 2008 Alton, IL

Position: Computer Programmer

Responsibilities:
- Developed Visual Basic frontend database applications, backend database SQL scripts, and Crystal Reports
- Interacted with users to determine program requirements

PRESENTATIONS

1. "Using M/G/1 Queueing Models with Vacations to Analyze Virtualized Logic Computations," Presented at the 33rd IEEE International Conference on Computer Design, New York, NY, USA, October 19, 2015.
2. "Utilizing Magnetic Tunnel Junctions in Digital Systems," Dissertation Defense, Presented in the Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, April 10, 2015.
3. "Performance Modeling of Virtualized Custom Logic Computations," Presented in the Doctoral Student Seminar, Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, March 7, 2014.
4. "Evaluating MTJ Benefits and Utilizing Context-Switched Hardware for Designing Magnetologic Circuits," Dissertation Proposal Defense, Presented in the Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, May 23, 2013.
5. "Building Virtualized Hardware Blocks in Digital Systems," Presented in the Doctoral Student Seminar, Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, November 13, 2012.
6. "Performance of a Resistance-To-Voltage Read Circuit for Sensing Magnetic Tunnel Junctions," Presented at the 55th IEEE International Midwest Symposium on Circuits and Systems, Boise, Idaho, USA, August 7, 2012.
7. "Approaches for Designing Context-Switched Deeply Pipelined Circuits," Presented in the Doctoral Student Seminar, Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, November 4, 2011.
8. "Noise Analysis of a Current-Mode Read Circuit for Sensing Magnetic Tunnel Junction Resistance," Presented at IEEE International Symposium on Circuits and Systems (ISCAS), Rio de Janeiro, Brazil, May 17, 2011.
9. "Design of a Current-Mode Read Circuit for Use in Magnetologic," Presented in the Doctoral Student Seminar, Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, September 10, 2010.
10. "Magnetic Random Access Memory (MRAM)," Oral Qualifications, Presented in the Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, November 11, 2009.
11. "Globally Clocked Magnetic Logic Circuits," Presented at IEEE International Magnetic Conference, Sacramento, CA, USA, May 5, 2009.
12. "An Introduction to Magnetologic," Presented in the Doctoral Student Seminar, Dept. of Computer Science & Engineering, Washington University in St. Louis, St. Louis, MO, USA, March 6, 2009.
13. "Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation," Masters Thesis Defense, Department of Electrical and Computer Engineering, Southern Illinois University Edwardsville, Edwardsville, IL, USA, December 13, 2007.
14. "Development of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Important", Presented in the Central States Universities

Incorporated Research Conference, held at Argonne National Laboratory, Lemont, IL, USA, November 2, 2007.

15. "Development of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Important", Presented at SIUE Graduate Student Research Symposium, Southern Illinois University Edwardsville, Edwardsville, IL, USA, April 3, 2007.

PUBLICATIONS

1. Hailey K. Hall, *An Aunt's Animal Alphabet*, Michael J. Hall, Ed. Hailey Kathleen Hall: St. Louis, 2023. [Online]. Available: https://www.haileyhall.art/aaaa-book
2. Michael J. Hall, Neil E. Olson, and Roger D. Chamberlain, "Utilizing Virtualized Hardware Logic Computations to Benefit Multi-User Performance," *Electronics* 2021, 10(6), 665, Mar 2021.
3. Michael J. Hall, Viktor Gruev, and Roger D. Chamberlain, "Characterization of a binary output resistance-to-voltage read circuit for sensing magnetic tunnel junctions," *IEEE Sensors Journal*, vol. 18, no. 3, pp. 1023–1031, Feb 2018.
4. Michael J. Hall, and Roger D. Chamberlain. "Using M/G/1 queueing models with vacations to analyze virtualized logic computations," in *2015 33rd IEEE Int'l Conf. on Computer Design (ICCD)*, Oct. 2015, pp. 78–85.
5. Michael J. Hall. "Utilizing Magnetic Tunnel Junction Devices in Digital Systems," Ph.D. dissertation, Dept. of Computer Science and Engineering, Washington University in St. Louis, May 2015.
6. Michael J. Hall, Roger D. Chamberlain. "Performance modeling of virtualized custom logic computations," in *Proc. of the 25th IEEE Int'l Conf. on Application-specific Systems Architectures and Processors (ASAP)*, Jun. 2014.
7. Michael J. Hall, Roger D. Chamberlain. "Performance modeling of virtualized custom logic computations," in *Proc. of the 24th ACM Int'l Great Lakes Symposium on VLSI*, 2014.
8. Michael J. Hall, Viktor Gruev, Roger D. Chamberlain. "Performance of a resistance-to-voltage read circuit for sensing magnetic tunnel junctions," *Circuits and Syst. (MWSCAS), 2012 IEEE 55th Int. Midwest Symp.*, August 2012.
9. Michael J. Hall, Viktor Gruev, Roger D. Chamberlain. "Noise analysis of a current-mode read circuit for sensing magnetic tunnel junction resistance," *Circuits and Syst. (ISCAS), 2011 IEEE*, May 2011.
10. Linda M. Engelbrecht, Albrecht Jander, Pallavi Dhagat, Michael J. Hall. "A toggle MRAM bit modeled in Verilog-A," *Solid-State Electronics*, vol. 54, no. 10, pp. 1135 – 1142, Oct. 2010. Selected Papers from ISDRS 2009.
11. Roger Chamberlain, Mark Franklin, Eric Tyson, James Buckley, Jeremy Buhler, Greg Galloway, Saurabh Gayen, Michael Hall, Berkley Shands, and Naveen Singla. "Auto-Pipe: Streaming applications on architecturally diverse systems," *Computer*, vol. 43, pp. 42 – 49, 2010.
12. George L. Engel, Michael J. Hall, Justin M. Proctor, Jon M. Elson, Lee G. Sobotka, Rebecca S. Shane, Robert J. Charity. "Design and performance of a multi-channel, multi-sampling, PSD-enabling integrated circuit," *Nuclear Instruments and Meth. A*, vol. 612, no. 1, pp. 161 – 170, 2009.
13. Raphael Njuguna, Michael Hall, and Vicktor Gruev. "Low power CMOS image sensor with programmable spatial filtering," in *IEEE Sensors 2009*, 2009, pp. 189 – 192.
14. Naveen Singla, Michael Hall, Berkley Shands, and Roger D. Chamberlain. "Financial Monte Carlo simulation on architecturally diverse systems," in *Workshop on High Perf. Comput. Finance, 2008. WHPCF 2008.*, 2008, pp. 1 – 7.
15. Michael J. Hall. "Design Considerations in Systems Employing Multiple Charge Integration for the Detection of Ionizing Radiation," M.S. Thesis, Dept. of Elect. Eng., SIUE, Dec 2007.

TECHNICAL SKILLS

Hardware:	Digital Design, FPGA Synthesis, PCB Design & Layout, IC Design & Layout, Digital Signal Processing, Microcontrollers, Soldering, Computer Networking
Languages:	C/C++, Visual C++, Visual Basic .NET, Python, Verilog, SystemVerilog, VHDL, SQL, Bash
Software:	Cadence IC design tools, PSpice, Xilinx Vivado, Intel Quartus, ModelSim, Synplicity, Mathcad, Mathematica, MATLAB, Python scientific libraries (numpy, scipy, matplotlib, pandas), Jupyter notebooks, Nginx, Django, PostgreSQL, Grafana, Prometheus, Jetbrain IDE tools (PyCharm, CLion, DataGrip, IntelliJ), SQL Server 2000, Git, Subversion, Windows (10, 7, XP, 2003 Server), FreeBSD, Linux, ZFS, Linux Containers (LXC), Docker, Docker Compose, Terraform, Adobe InDesign, Gimp, WordPress