Globally Clocked Magnetic Logic Circuits

Michael Hall
Albrecht Jander
Roger D. Chamberlain
Pallavi Dhagat

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Dept. of Computer Science and Engineering
Washington University in St. Louis

and

School of Electrical Engineering and Computer Science
Oregon State University

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M. Hall[1], *A. Jander*[2], R. D. Chamberlain[1], P. Dhagat[2]
1. Computer Science and Engineering, Washinton University, St. Louis, MO; 2. Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR

We have investigated a magnetic logic device and architecture that uses an externally applied, ac magnetic field as a global clock signal for the circuit. The use of a wireless, globally distributed clock reduces the routing and power required for on-chip clock distribution and eliminates any possibilities of clock skew. The clock field, applied along the hard axis of the magnetic device, dynamically reduces the switching threshold so that low-gain magnetoresistive devices can, in principle, be cascaded without intervening semiconductor amplifiers. The enabled latches can be configured to respond to either a positive or negative clock field, allowing them to be configured in a two-phase master/slave flip-flop appropriate for sequential logic circuits.

In current integrated circuits, as much as 40% of chip area [1] and as much as 40% of power consumption [2] may be attributed to clock distribution. As integration densities increase, these percentages are likely to increase and the problem of clock skew due to delays in the clock signals propagating from one part of the chip to another will become more severe. A digital latch which is clocked by an externally applied, global signal could dramatically reduce on-chip power dissipation, reduce routing complexity and eliminate clock skew in future integrated circuits.

A master/slave flip-flop comprised of two enabled transparent latches is illustrated in Fig. 1. The structure of each latch is similar to a spin valve MRAM cell. The data line (D) and enable line (EN) generate fields in the easy axis and hard axis directions of the spin valve respectively. In addition, there is an externally applied magnetic field (clock) that adds to the hard axis field. Operation of the latch is illustrated with the Stoner-Wohlfarth switching astroids for the spin valves. The possible magnetic field vectors that can be seen by the spin valve due to the current in the D, EN and the external bipolar clock field are indicated by the constellation of symbols. To allow unipolar currents in the data line, the easy axis field is offset using an internal bias field in the spin valve. A low current (D=0) in the data line leaves the net field in the left half of the astroid. A high current (D=1) makes the net field positive in the easy axis direction. The magnitude of the enable current and external clock field are chosen so that each alone will not result in a field outside of the stable region in the astroid. With enable low, the field can reach only the square points within the astroid. Only when the clock is on AND enable is on can the field reach the diamond points outside of the switching threshold and cause the latch to switch its magnetic state according to the current value of the D input. For the master latch, this occurs when the external clock field is negative. The slave latch is switched when the clock field is positive. This gives us the classic function of a master-slave flip-flop. The flip-flop has an advantage over traditional CMOS master-slave designs which are susceptible to errors if the two clock polarities are not correctly phase aligned. Since the proposed magnetic latch is clocked by a single bipolar clock, it can not experience clock skew between phases of the clock.

Despite recent advances in tunneling magnetoresistance technology, the best on:off resistance ratios of current spin valve devices are still only about 2:1, making it difficult to achieve large changes in output current with magnetic logic devices. An advantage of the externally clocked latch is that the clock field dynamically reduces the switching threshold so that low current levels are sufficient to switch the slave device directly with the master output as shown in Fig 1. The power required to generate the clock field is not dissipated on chip. We have demonstrated the operation of the latch and the dynamic threshold reduction using a discrete spin valve with a built-in easy-axis offset of 17 Oe. Shown in Fig. 2 is the probability of switching to the "1" state by a hard axis clock pulse as a function of the easy axis field. With a saturating hard axis pulse, the device is switched reliably with only 2 Oe field differential as opposed to the original 50 Oe switching field.

The devices described above are enabled memory elements, but their design does not preclude the inclusion of logic functions within the same device. If, instead of a single D input, there are multiple data lines, combinational logic functions AND and OR may be constructed [3].

[1] Y. Cheon et al., Proc. Design Autom. Conf, 795 (2005)

[2] D. Duarte et al., Proc. of IEEE Comp. Soc. Ann. Symp. on VLSI, (2002)

[3] A. Ney et al., Nature, 425, 485 (2003)

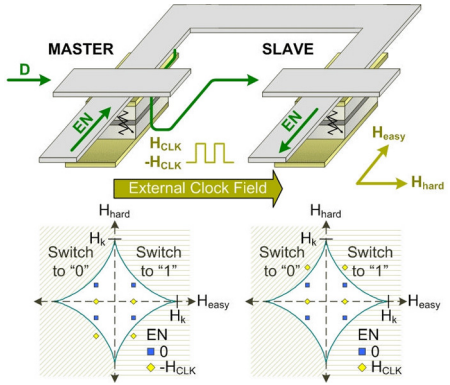

Fig. 1.

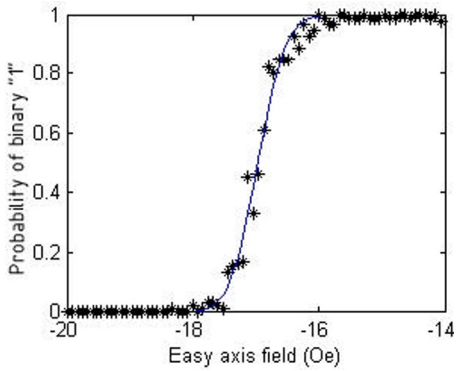

Fig. 2.