Development of a Multi-Channel Integrated Circuit for Use in Nuclear Physics Experiments Where Particle Identification is Important

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Design Team

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Western Michigan:

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Research Objective

- Design a custom microchip which can be used by nuclear physicists when they perform experiments.
- In these experiments, physicists use detectors to sense radiation.
- These experiments often require that the physicists identify the type of radiation (α particle, γ-ray, etc) that struck the detector.

NSF Proposal (Funded)

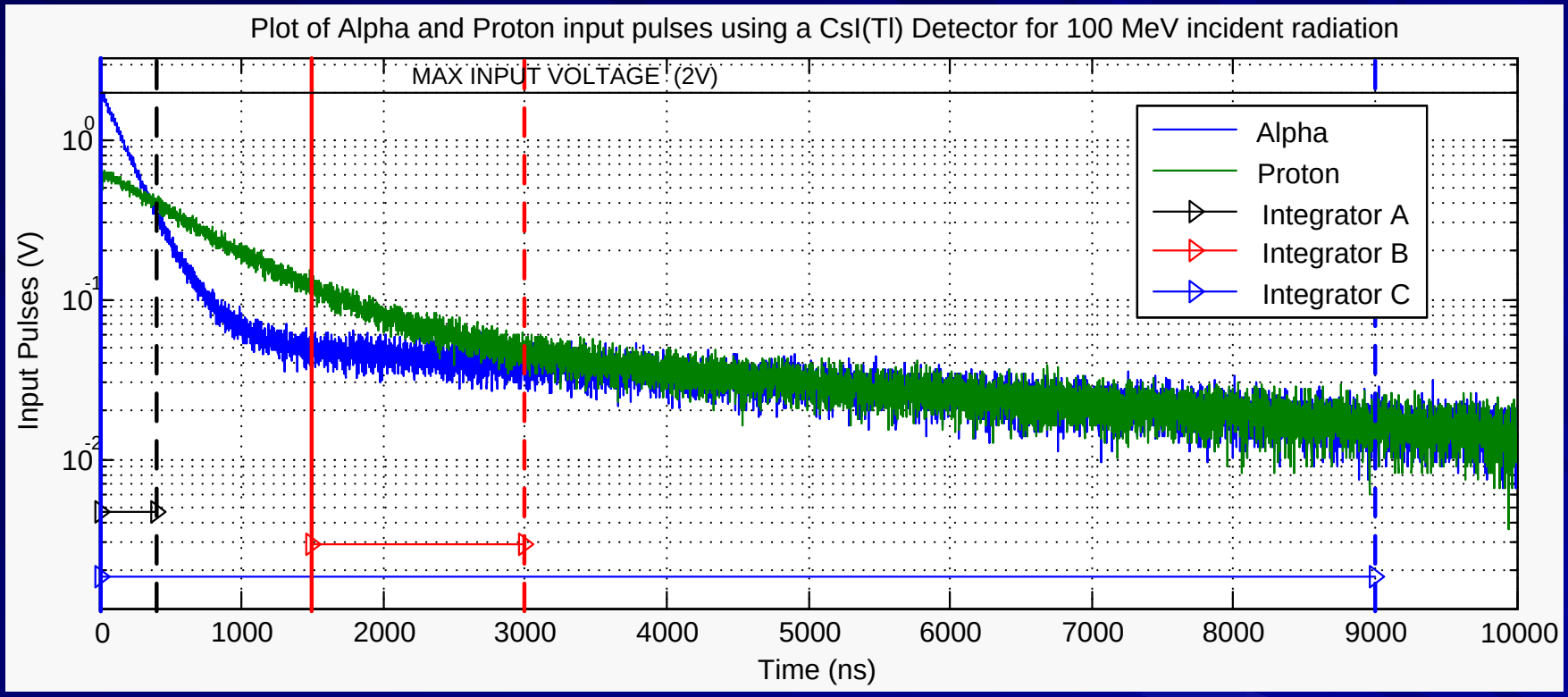
- $200,000 grant funded from September 2006 to August 2008.
- Design, simulate, and fabricate a custom integrated circuit for particle identification suitable for use with
  - CsI(Tl) (used for charge-particle discrimination)
  - Liquid Scintillator (used for neutron-gamma discrimination)
- 8 channel “prototype” chip
- 16 channel “production” chip

Intended Applications

- The chip will be used in an experiment at the National Superconducting Cyclotron Laboratory (NSCL) in Fall 2008 by Washington University collaborators.

- Mass production of PSD technology is actively being sought by our government's Department of Homeland Security.

Simulated Input Pulse for CsI(Tl) Detector

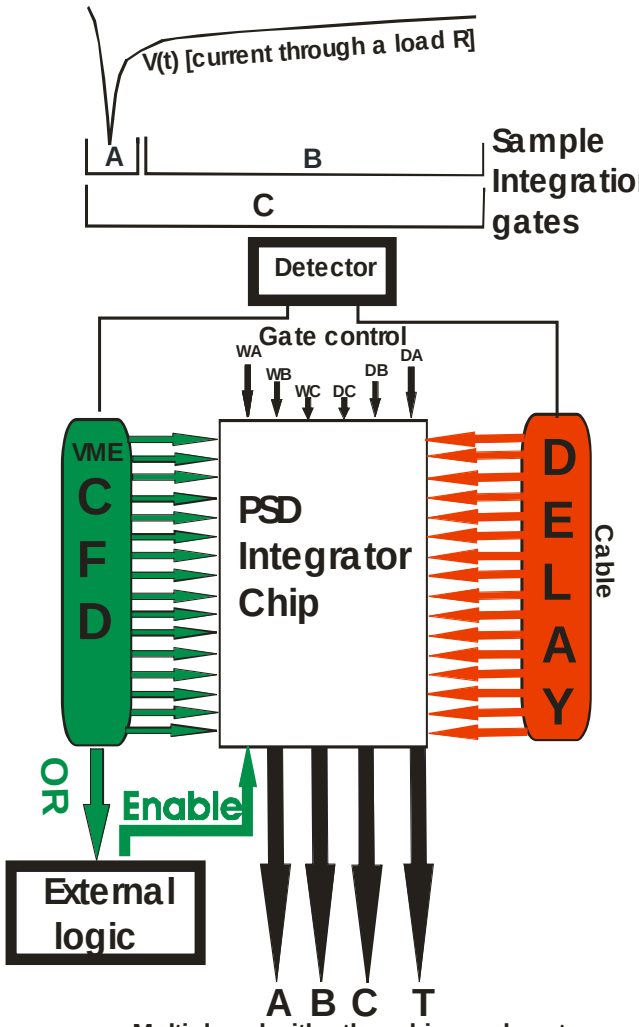


- Integrators
  - A 0 to 400 ns
  - B 1500 to 1500 ns
  - C 0 to 9000 ns
- Integration periods at the beginning of the signal are assumed to start before the pulse (at -5 ns).

Need for an Integrated Circuit

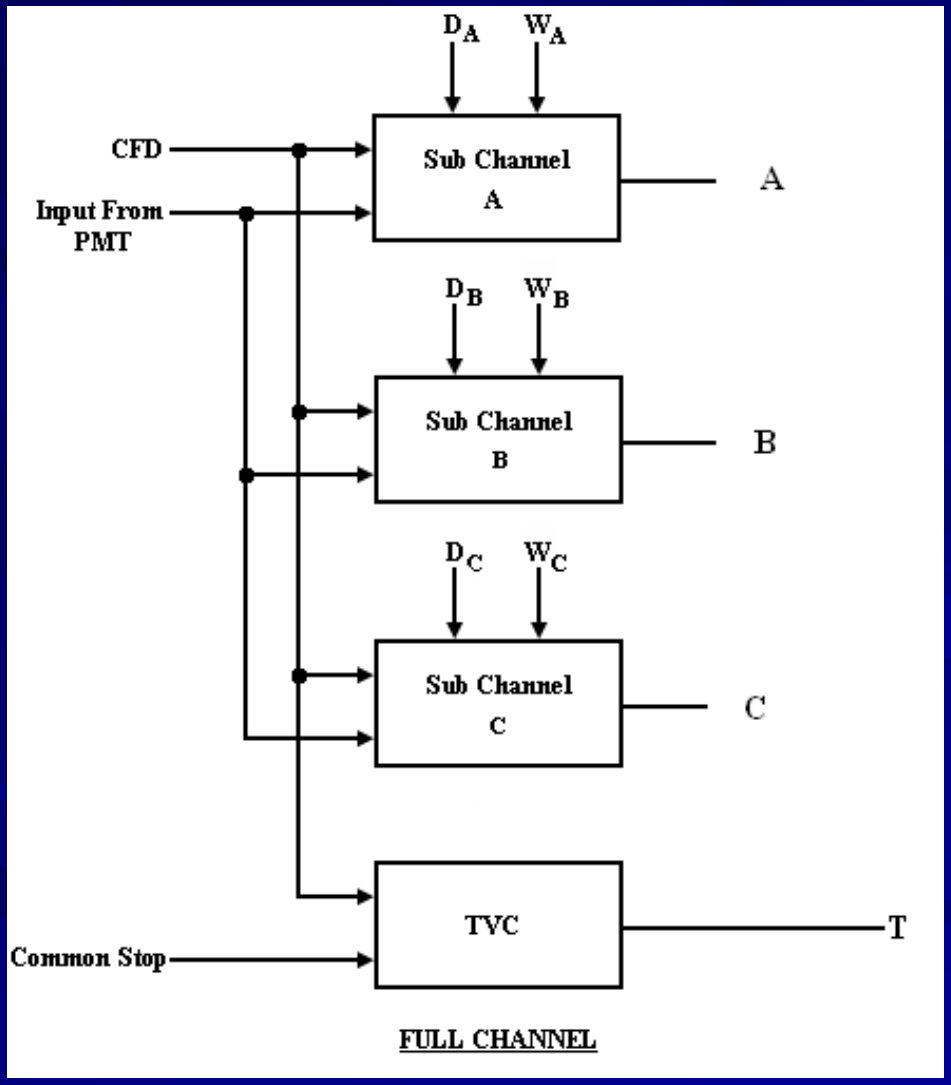
- Particle identification (α particle, γ-ray, *etc.*) capability
- Ability to support multiple (*i.e.* initially eight but eventually sixteen) radiation detectors
- Three separate integration regions with independent control of charging rate in each region which can be used for high-quality pulse shape discrimination (PSD).
- Built-in high-quality timing circuitry
- Multiple (3) triggering modes
- Data sparsification

Overview of PSD System



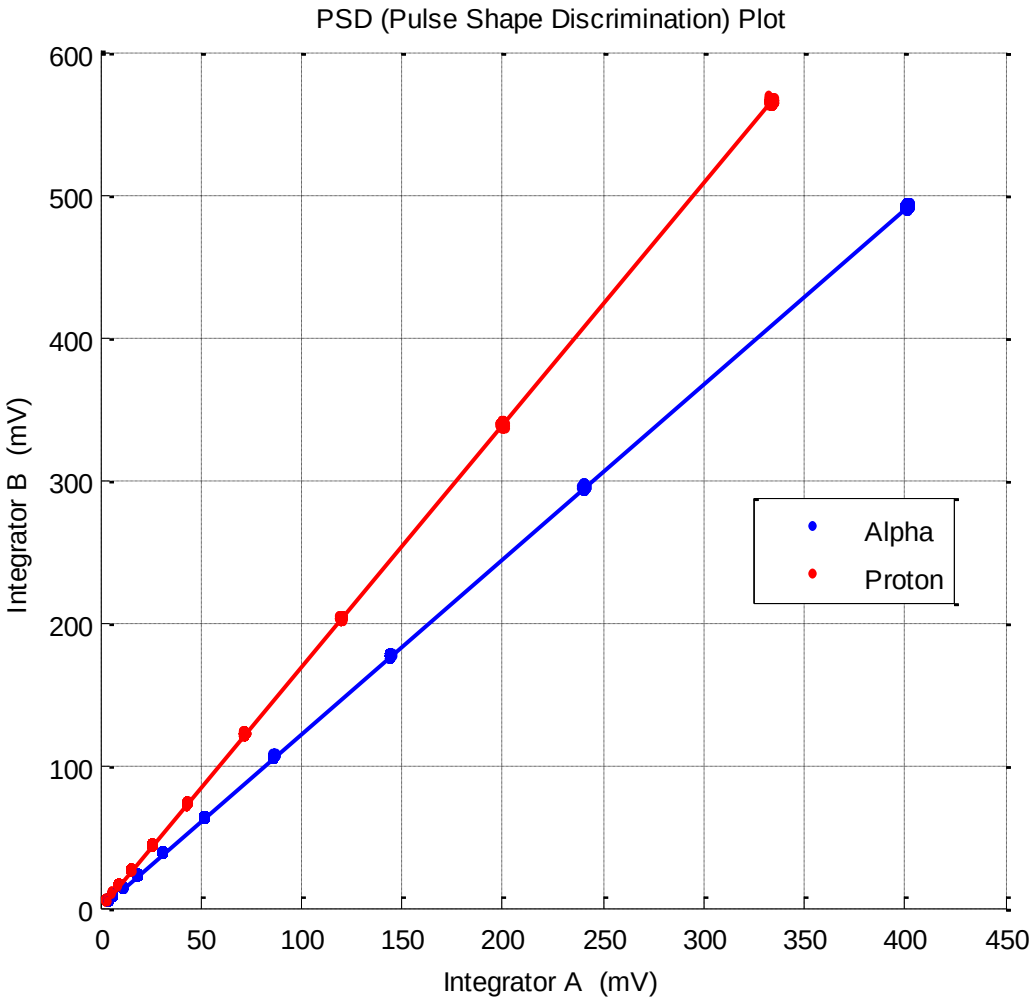
- Detector (PMT or photodiode)
- External discriminators (CFDs)
- External delay lines so we can start integrations before arrival of pulse
- External control voltages determine Delay and Width of integration periods
- Outputs A, B, C integrator voltages and relative time, T

Channel



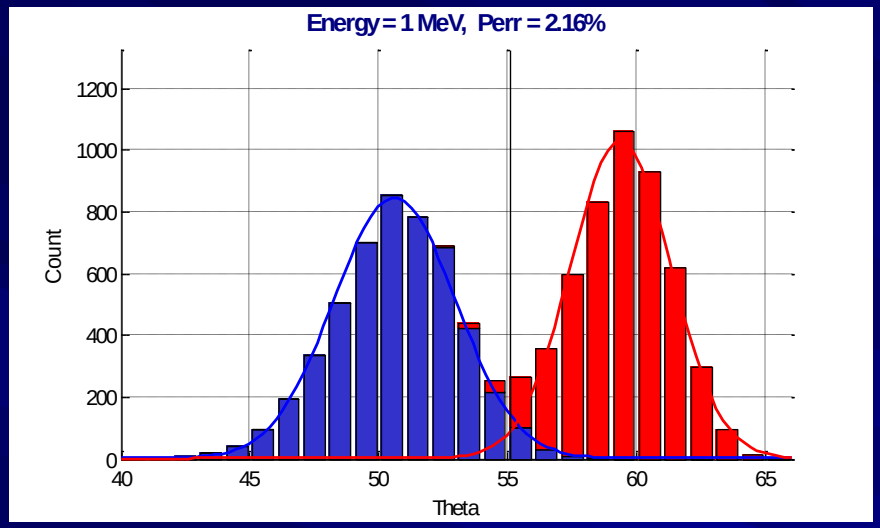
- 3 on-chip sub-channels for integrators A, B, C
- Delay and width of integrators set by externally supplied control voltages
- Timing relative to a common stop signal

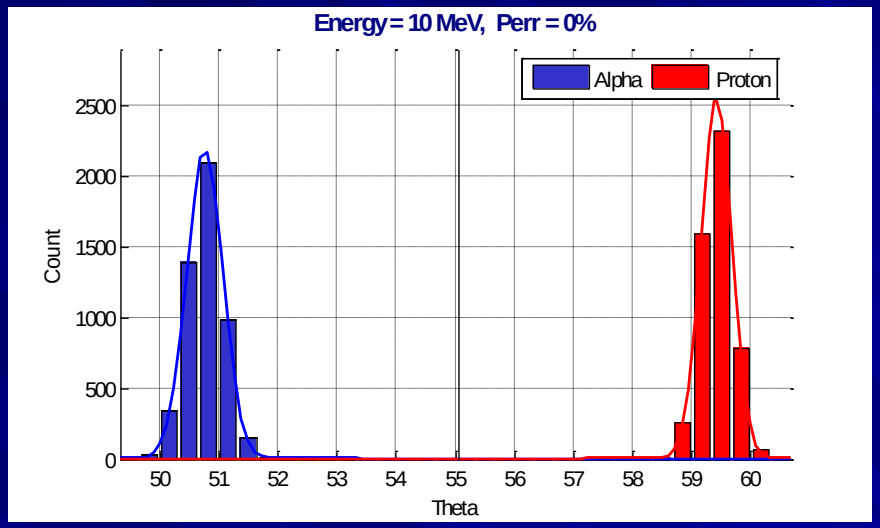
Pulse Shape Discrimination Plot for CsI(Tl) Detector

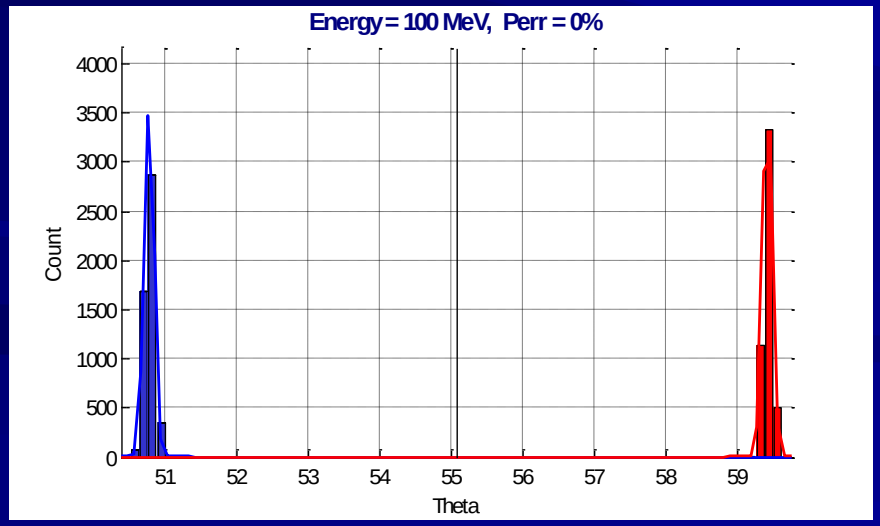


- Detector: CsI(Tl)
- Integrators: A, B
- Energy Max: 100 MeV (for 2V at input of integrator)
- Energy Range: 1 – 100 MeV
- Includes all noise sources

Angular PSD Plots (CsI)

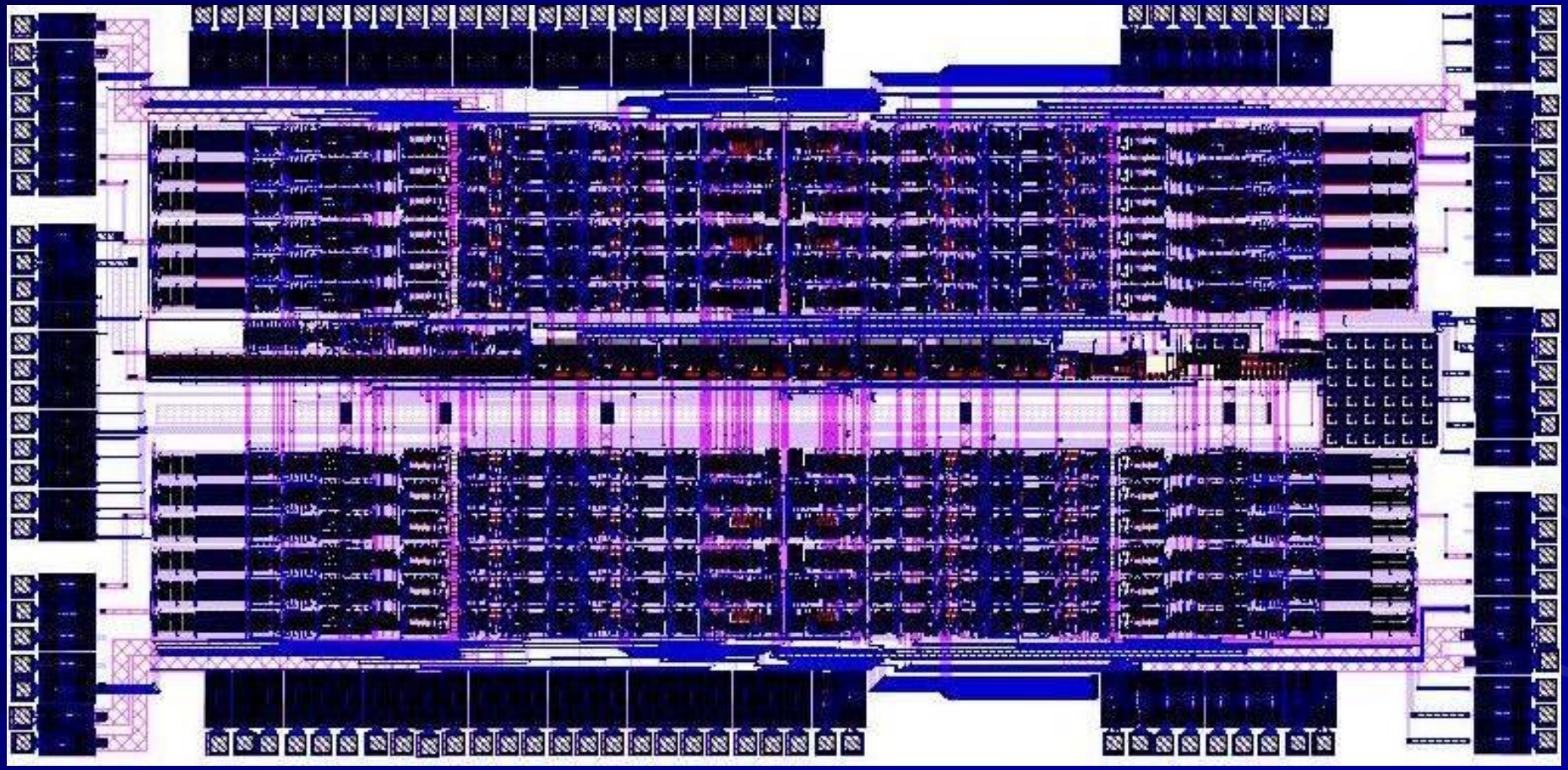






- Detector: CsI(Tl)
- Integrators:
  A, B
- Energy Max:
  100 MeV
- Energy Range:
  1 – 100 MeV
- 5000 realizations
- Includes all noise sources

PSD Chip



Current Work

- High level simulations to verify chip functionality

Future Work

- Fabrication
  - Chip should leave for fabrication in November 2007.
  - Will take approximately 2 months to make.
- Testing of the IC
- Chip will be used in experiment at NSCL in Fall 2008