Magnetic Random Access Memory (MRAM)

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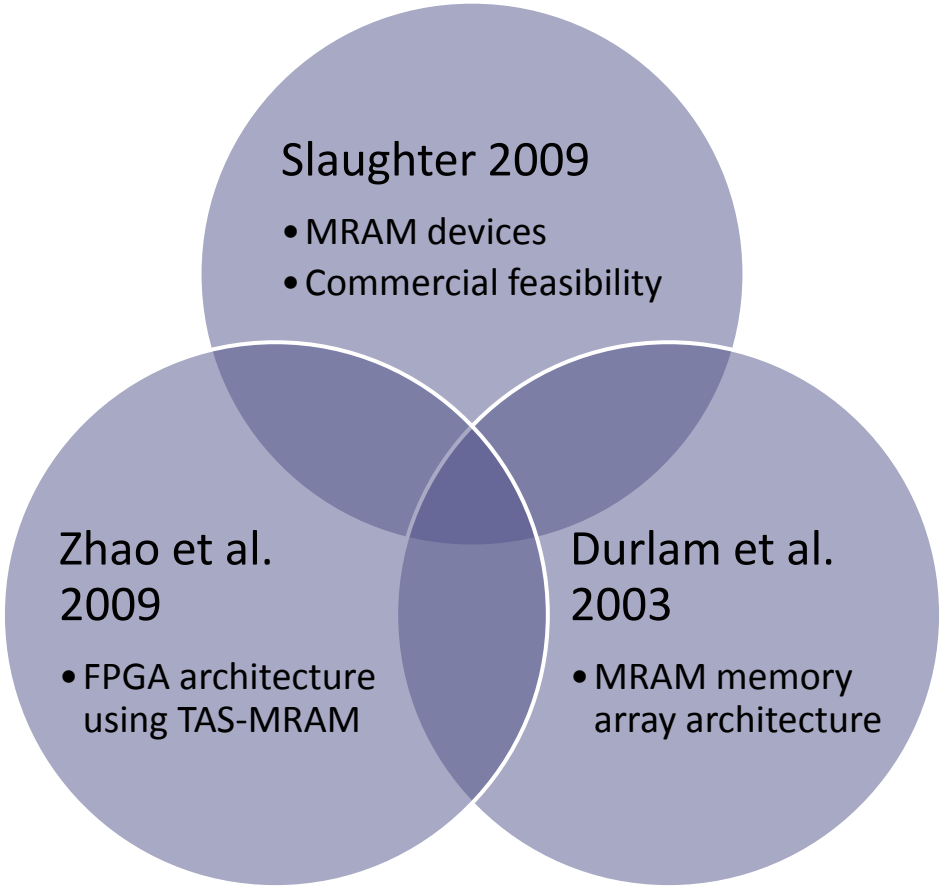
Paper Choices



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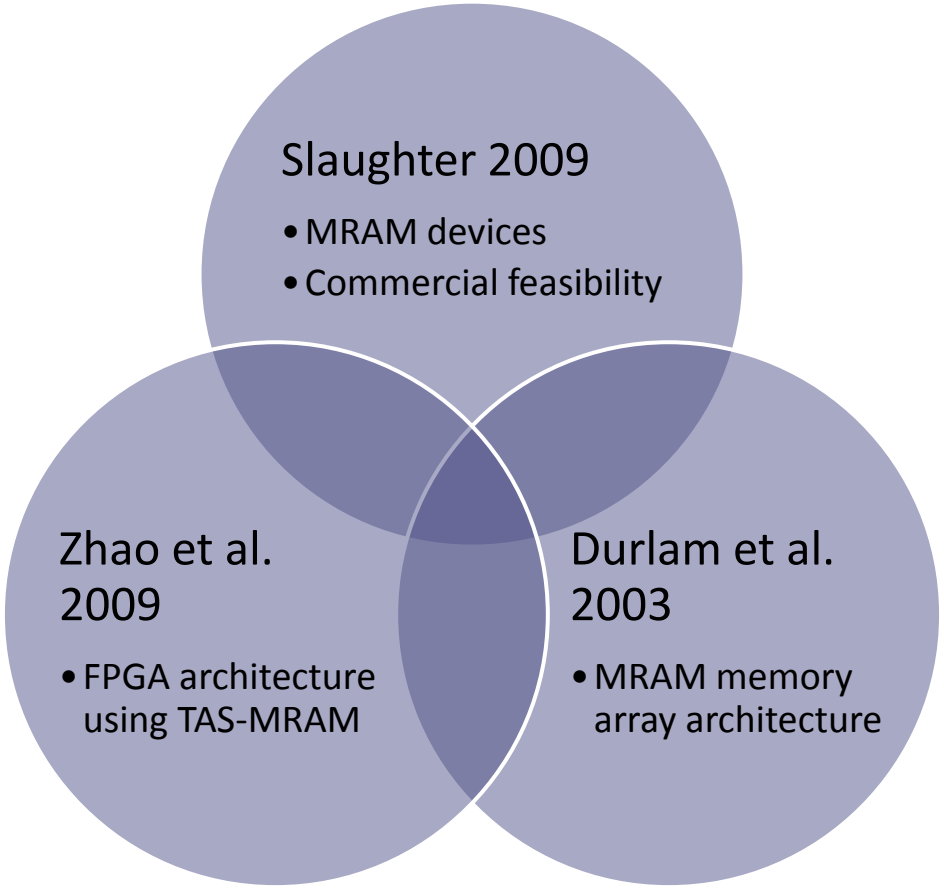
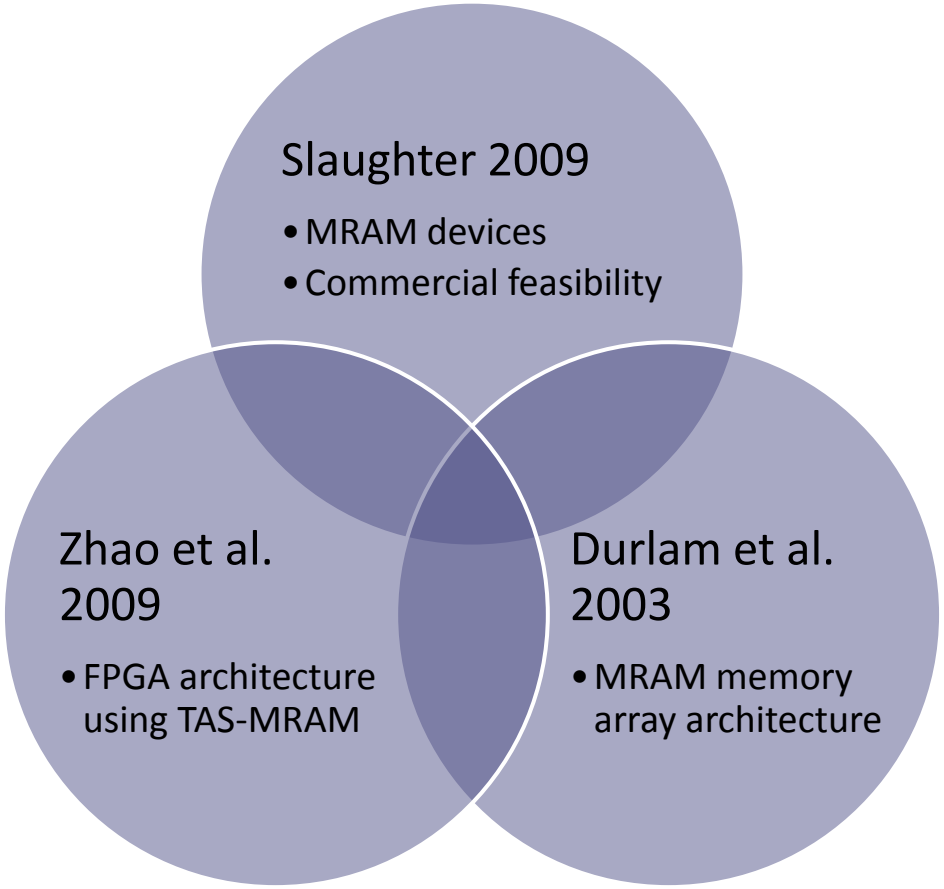


Goals

- To build commercially feasible memory and FPGA circuits

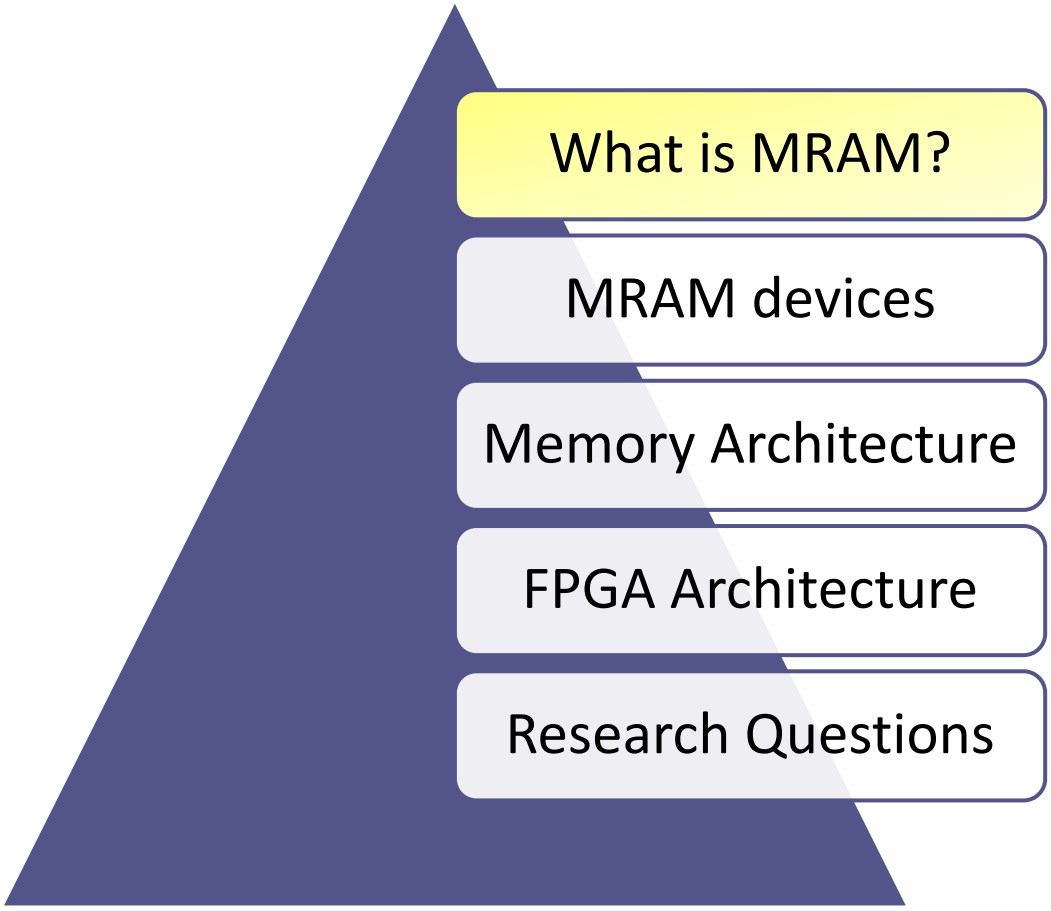
Paper Choices



Goals

- To build commercially feasible memory and FPGA circuits
- To discuss existing research efforts
- To identify potentially new research areas

Outline


What is MRAM?
MRAM devices
Memory Architecture
FPGA Architecture
Research Questions

What is MRAM?

- Magnetic Random Access Memory (MRAM)
- Operates using principles in thin-film magnetics
- Potential to compete with existing memory technologies (eg. DRAM, SRAM) in terms of power and speed

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- Nonvolatile
- No static power dissipation
- High write endurance (> 10^{15})
- High density

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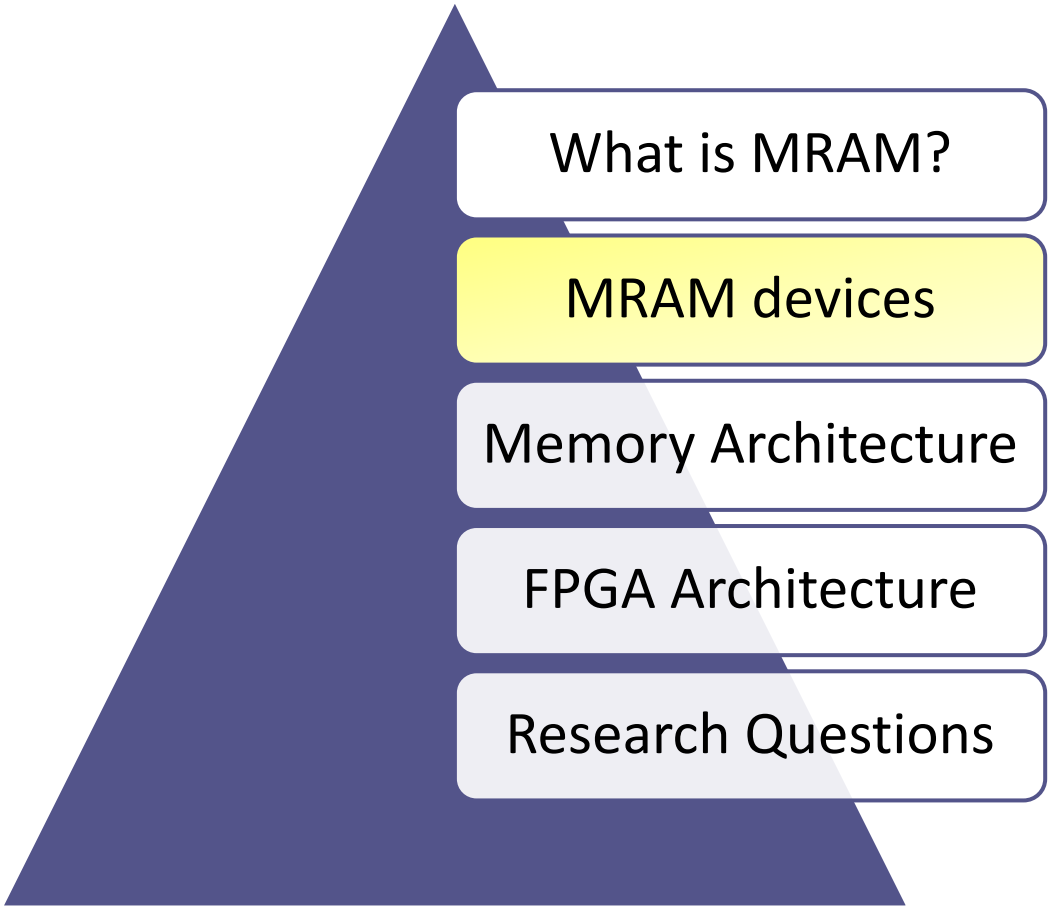
Goals for MRAM devices

- Higher speed
- Lower power
- Higher reliability
- Scalable

Outline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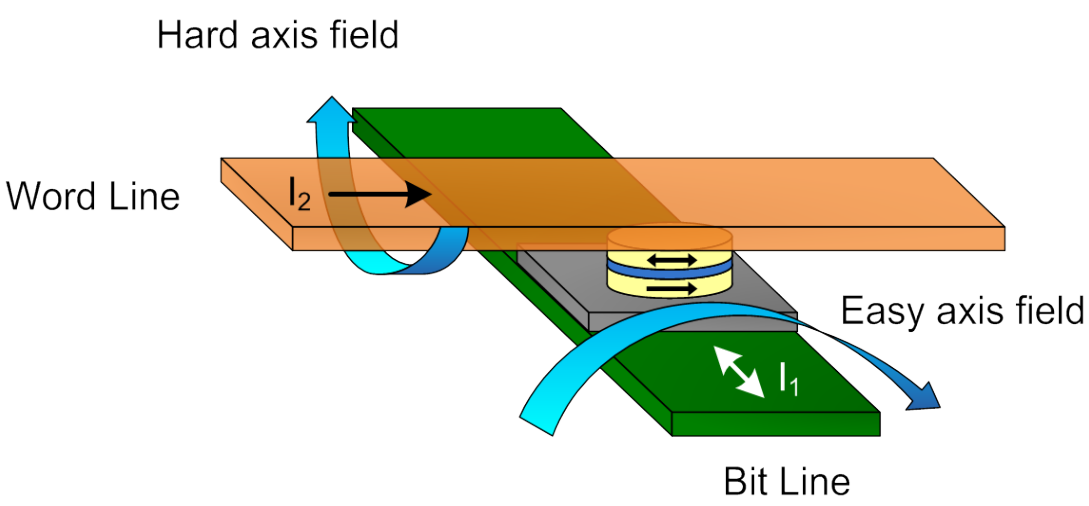
Conventional MRAM (FIMS)



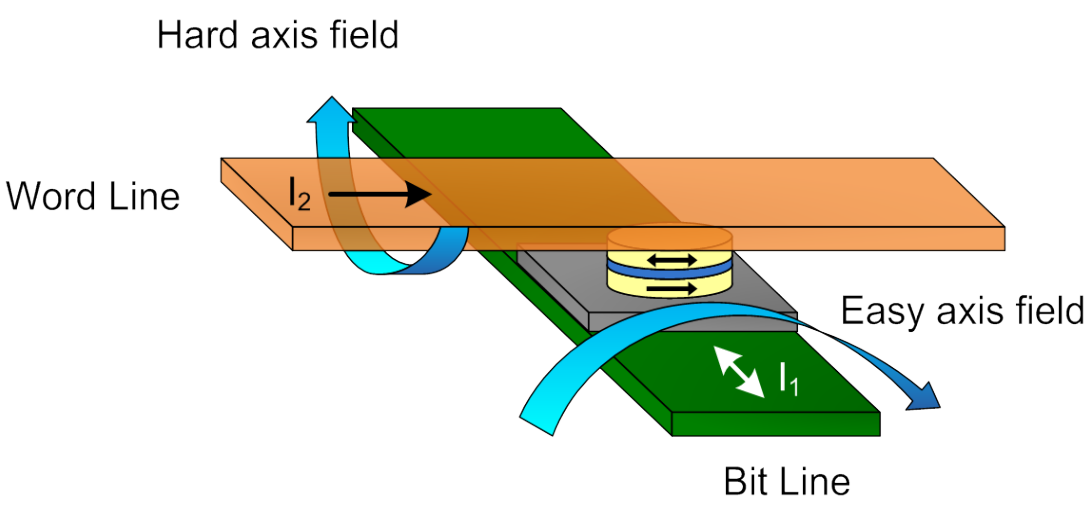
Material Stack

Electrode
Free layer
Insulator
Pinned layer
AF pinning layer
Electrode

- Uses field-induced magnetic switching (FIMS) using currents through perpendicular conductors
- High power consumption (large write currents)
- Unidirectional word line current
- Bidirectional bit line current

Durlam 2003

Conventional MRAM (FIMS)



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Durlam 2003

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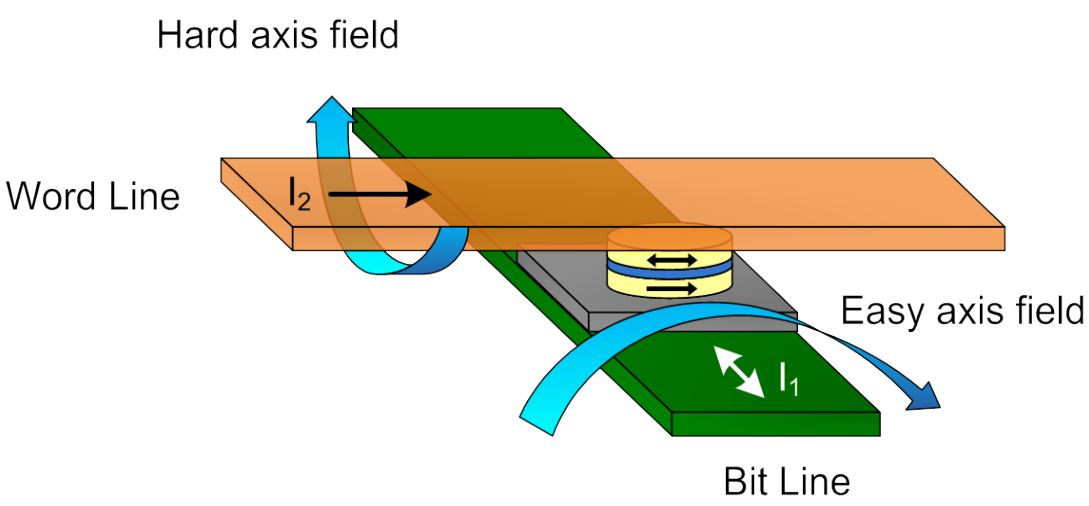

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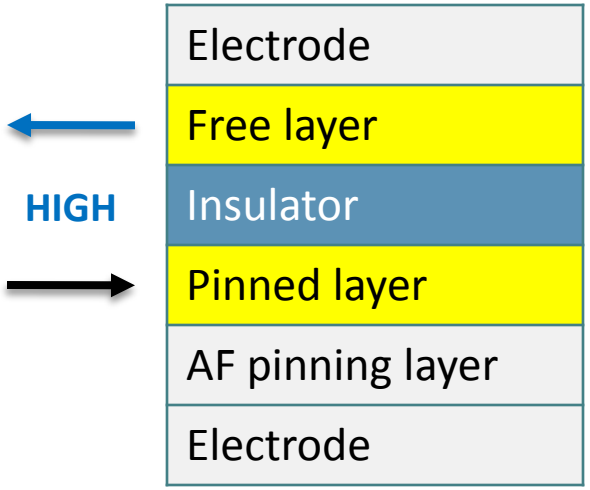

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Durlam 2003

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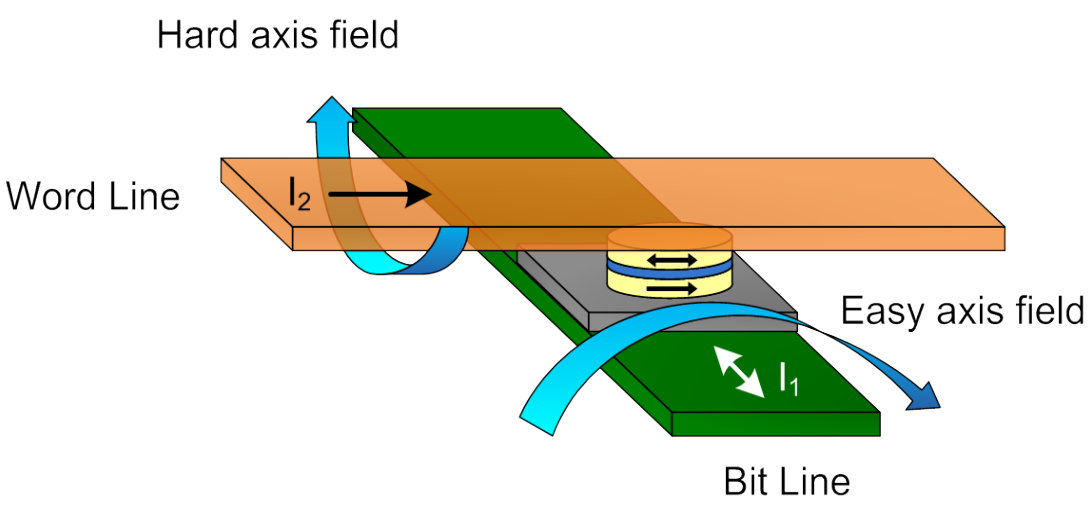

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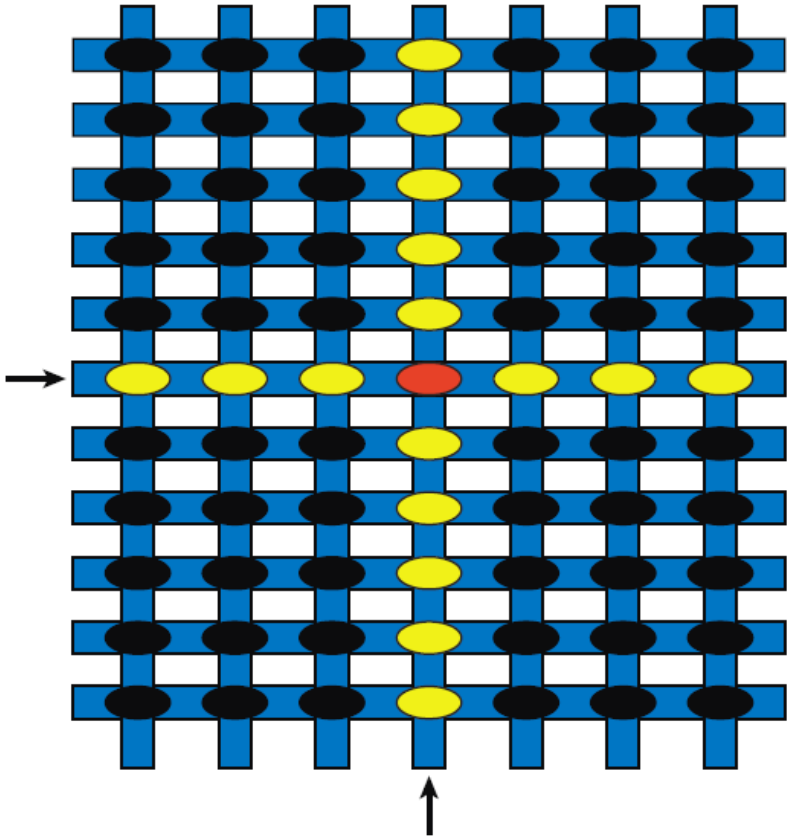
Durlam 2003

Half-Select Problem

- In a memory array, a cell is selected by driving current into the word line for a row and the bit line for an column.
- The selected device is at the intersection of the row and column.
- All other devices in the same row or column are half-selected.



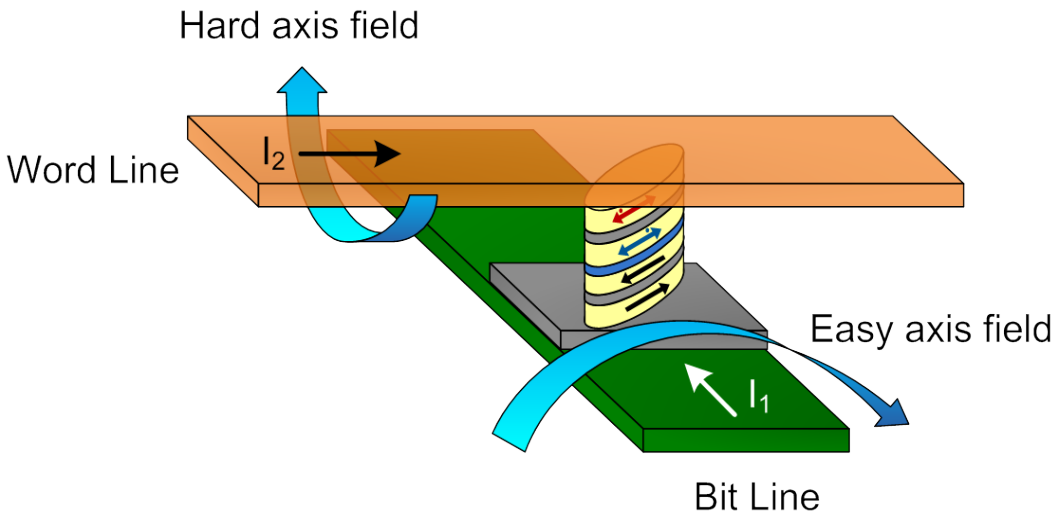
Slaughter 2009

Memory Technologies

					FPGA	
Tech.	**Energy**	**Area**	**Speed**	**Memory**	**Config.**	**Flip-Flop**
FIMS	1.2 nJ		Less than 50 ns (1)			
SRAM	0.151 nJ	146 F^2	4.7 ns			
DRAM	0.570 nJ	21 F^2	5.8 ns			
Flash		< 21 F^2				

(1) This time is for an entire write cycle to memory.

Toggle MRAM



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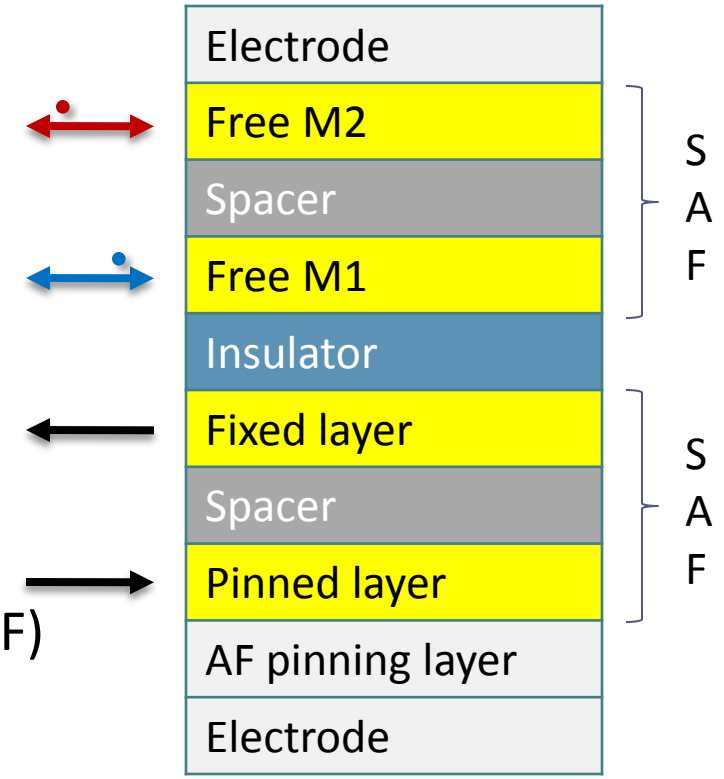

- Built using a Synthetic Antiferromagnetic (SAF) layer which consists of two ferromagnetic layers separated by a non-magnetic spacer
- A write toggles the output state
- Unidirectional write currents
- No half-select problem

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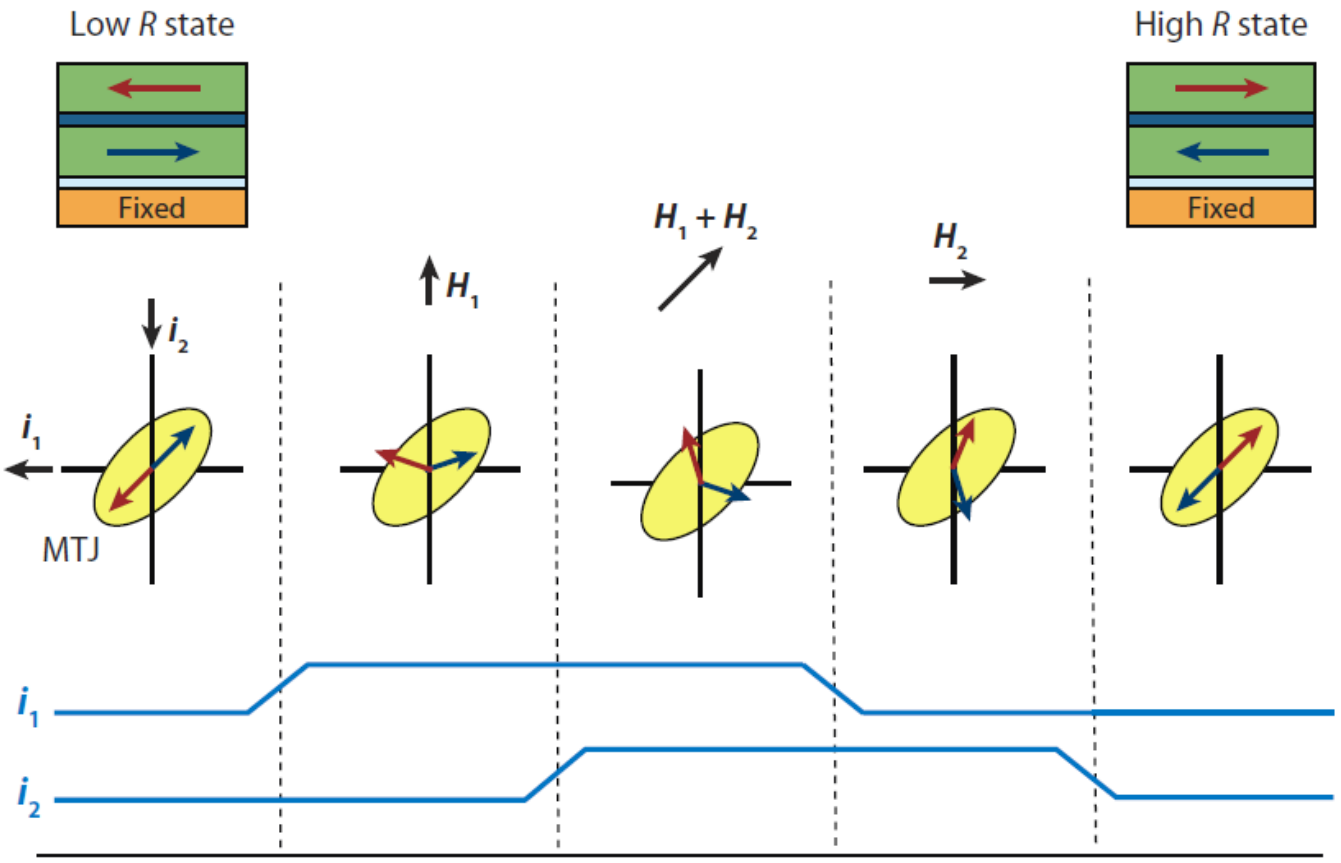

Figure 12

Schematic of a toggle MRAM bit with the field sequence used to switch the free layer from one state to the other. The fields, H_1, $H_1 + H_2$, and H_2, are produced by passing currents, i_1 and i_2, through the write lines.

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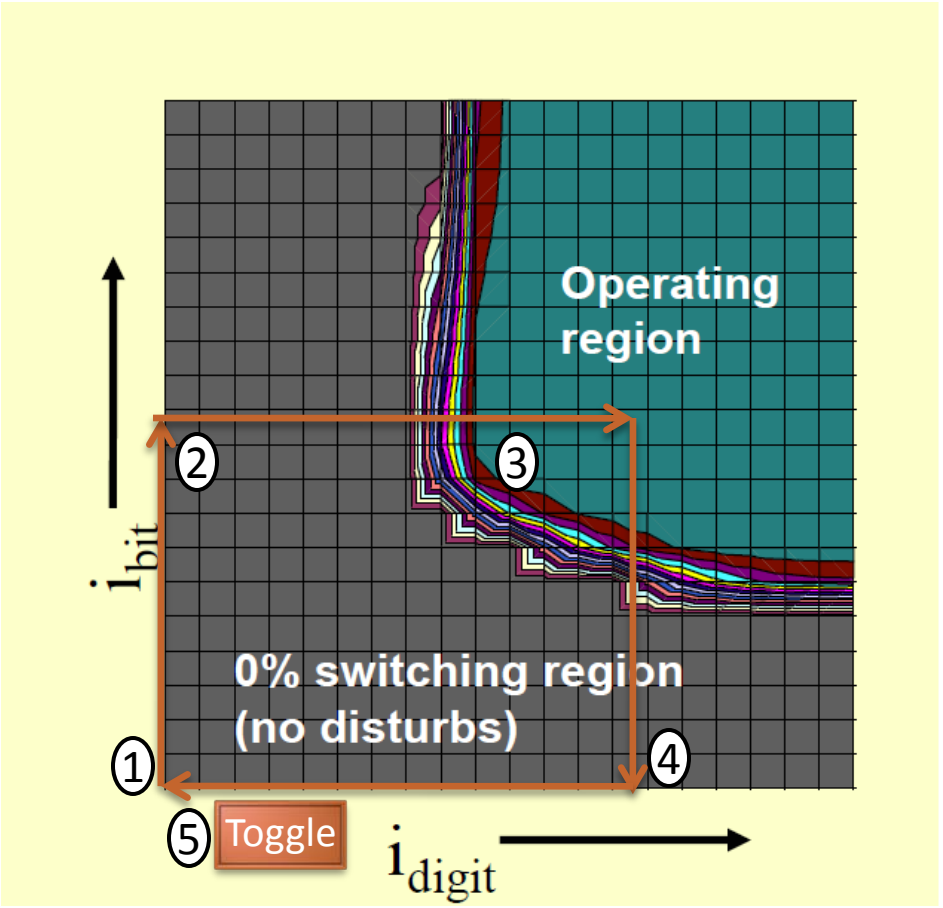
Toggle MRAM

- Measured switching from 4Mb Toggle-MRAM test chip
- No single field along one axis will cause a toggle to occur



Slaughter 2004 Presentation

Memory Technologies

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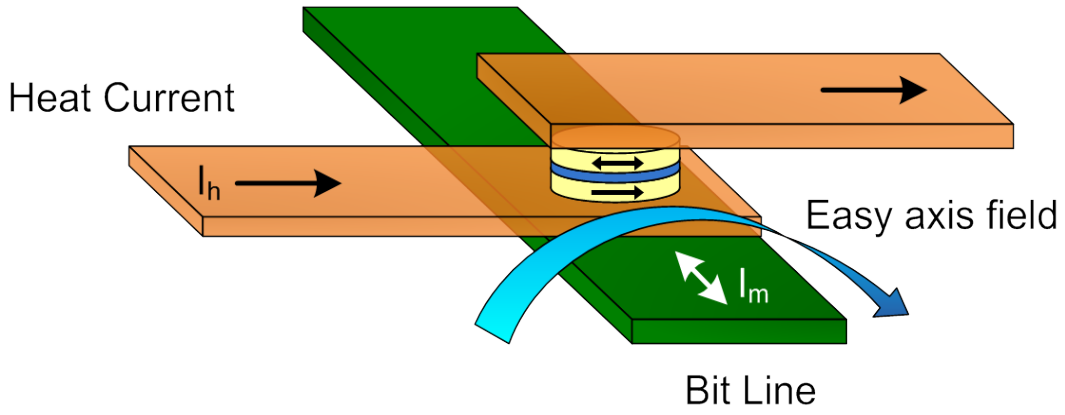
TAS-MRAM



Material Stack

Electrode
AF pinning layer (Lower T_{B2})
Free layer
Insulator
Pinned layer
AF pinning layer (Higher T_{B1})
Electrode

- Unidirectional heat current
- Bidirectional bit line current
- Very low power consumption
- Slow write times

Zhao 2009

Memory Technologies

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FIMS	1.2 nJ		Less than 50 ns (1)			
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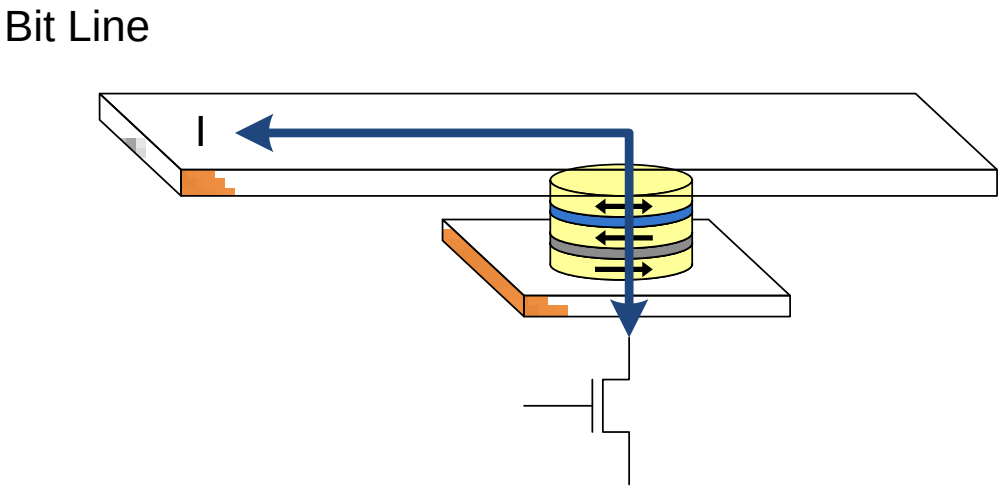
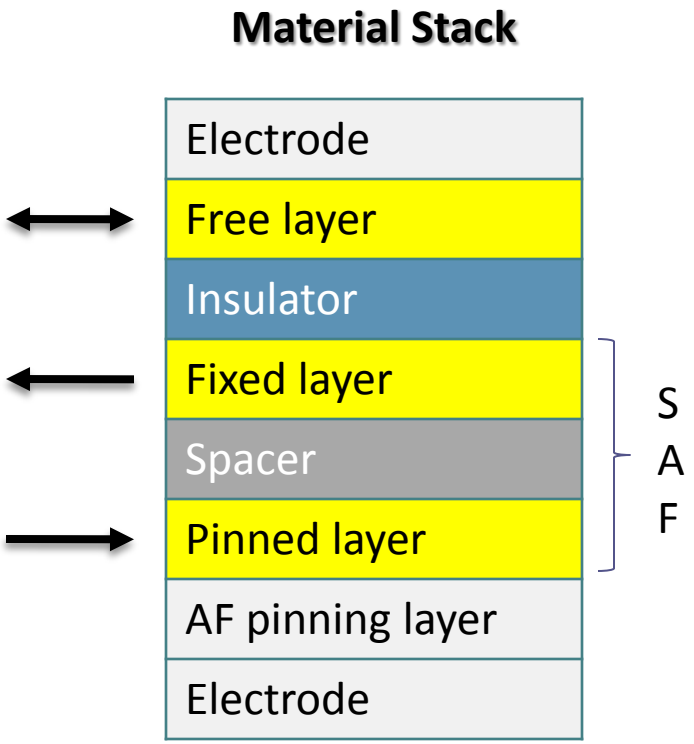
STT-MRAM





- Bidirectional write current
- Fast write times
- Power scales favorably with process dimensions

Memory Technologies

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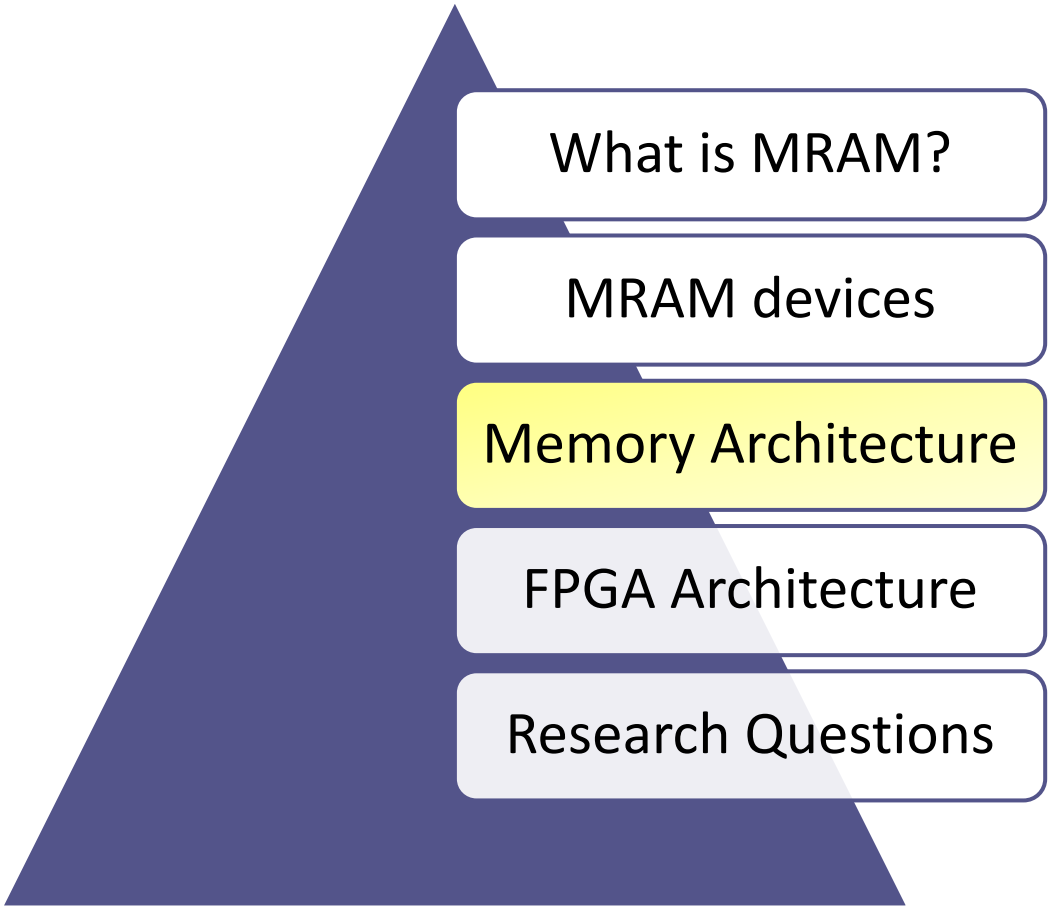
Outline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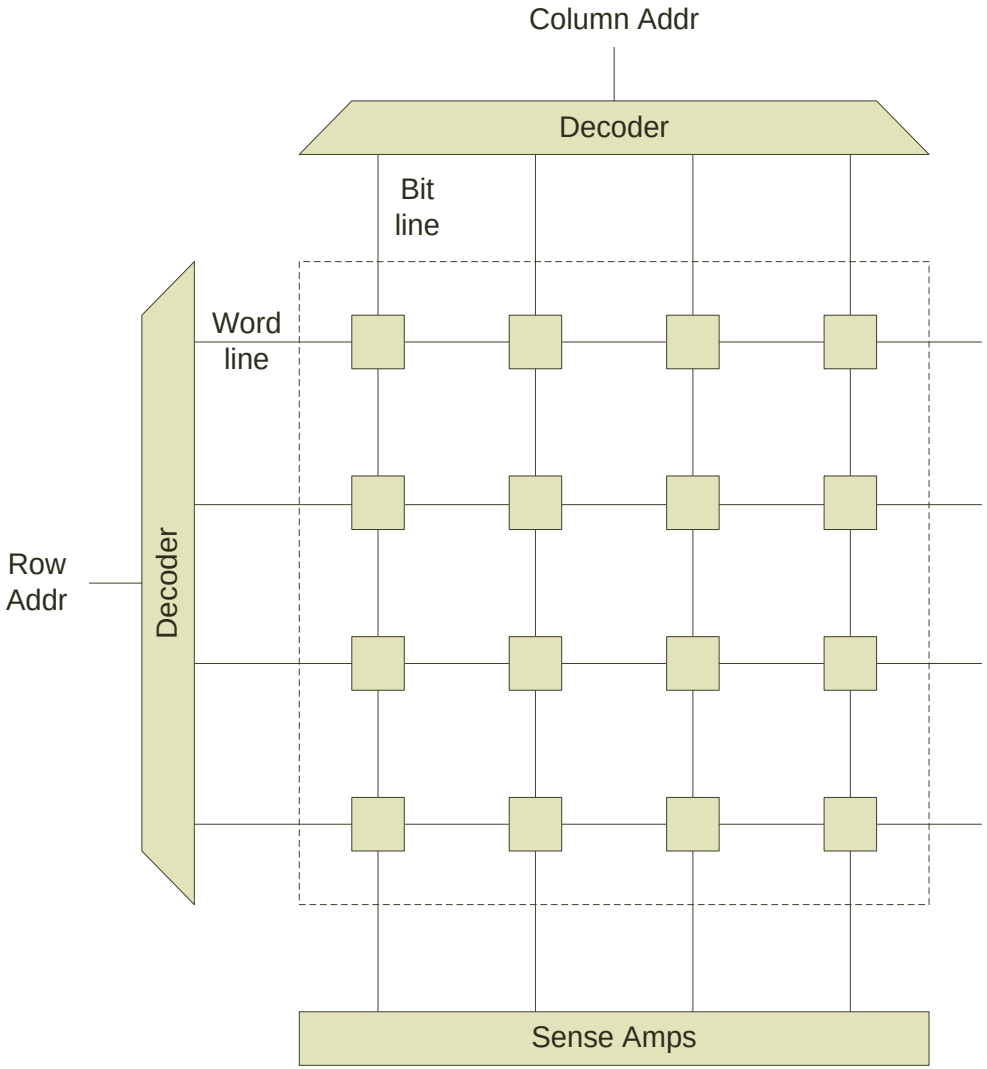
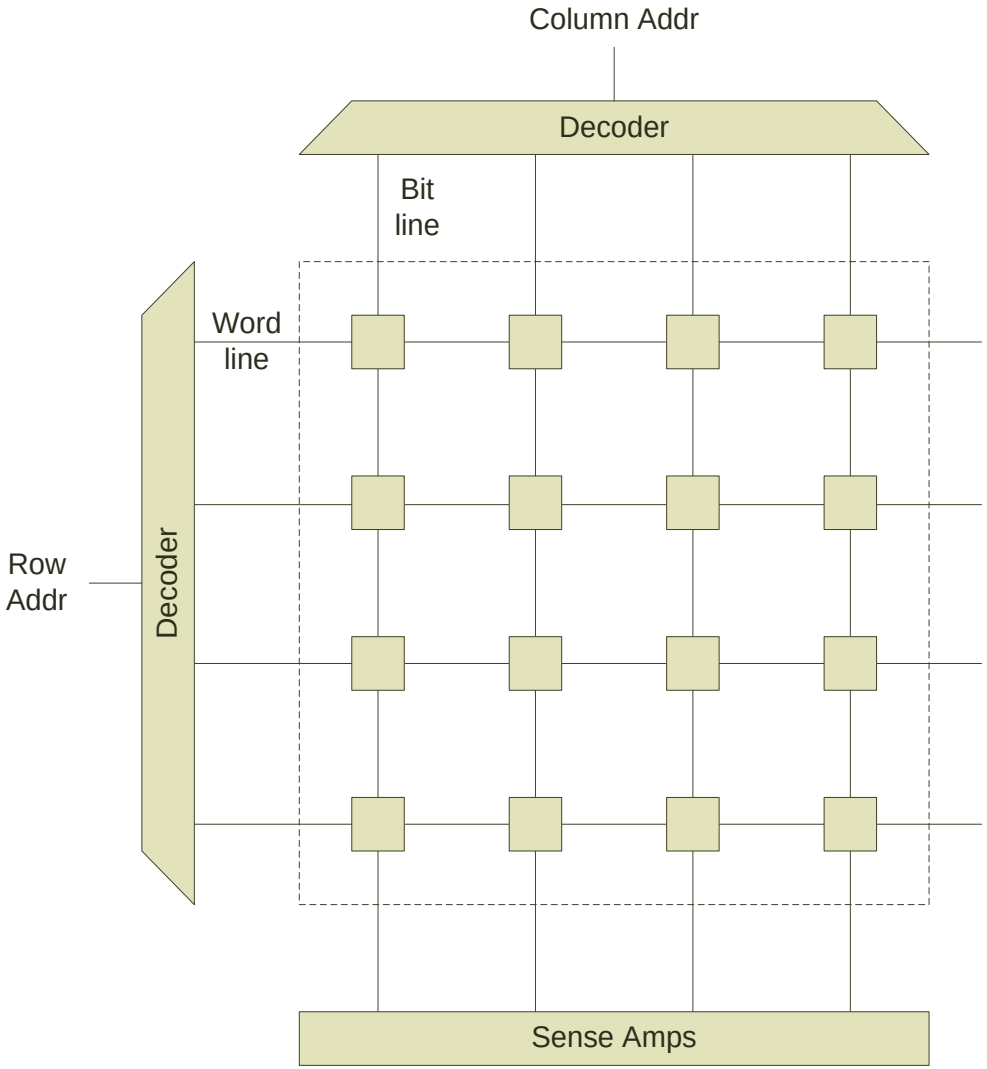
Memory Architecture

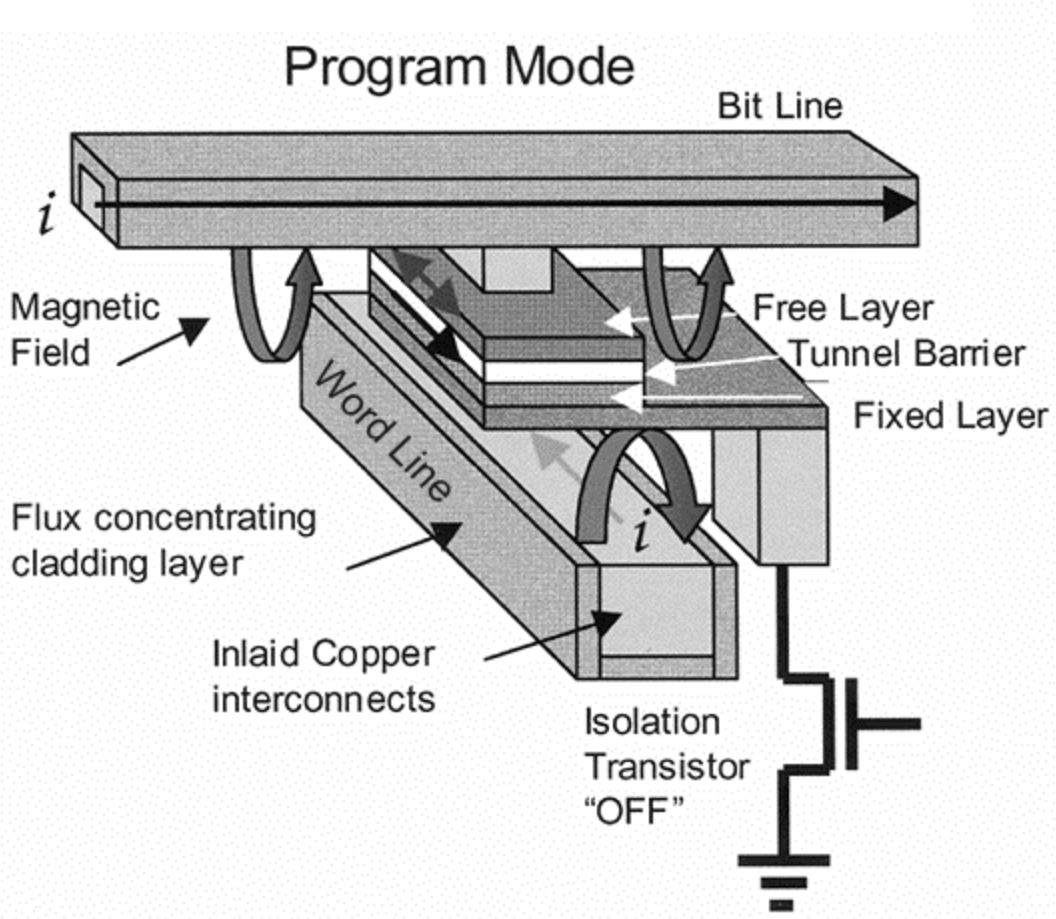


Memory Architecture



- MRAM uses the same architecture. The difference is in the details.
- Durlam in 2003 presented a 1-Mb test chip of an MRAM memory array using a 1T1MTJ cell

1T1MTJ cell (FIMS)



- Consists of:
  - Word and bit line
  - MTJ
  - Isolation transistor
- Flux-concentrating cladding focuses magnetic field

Durlam 2003

Sense Amplifier

- Compares the resistance state of the MTJ to a reference value
- A reference cell creates a midpoint resistance between high and low states using 4 MTJs in a series-parallel combination.
- The sense amplifier clamps the voltage across the MTJ device in both the reference circuit and the memory array using a pair of current conveyors.
- The read current and reference current form a differential signal pair which is boosted and converted to a voltage.

1-Mb Test Chip

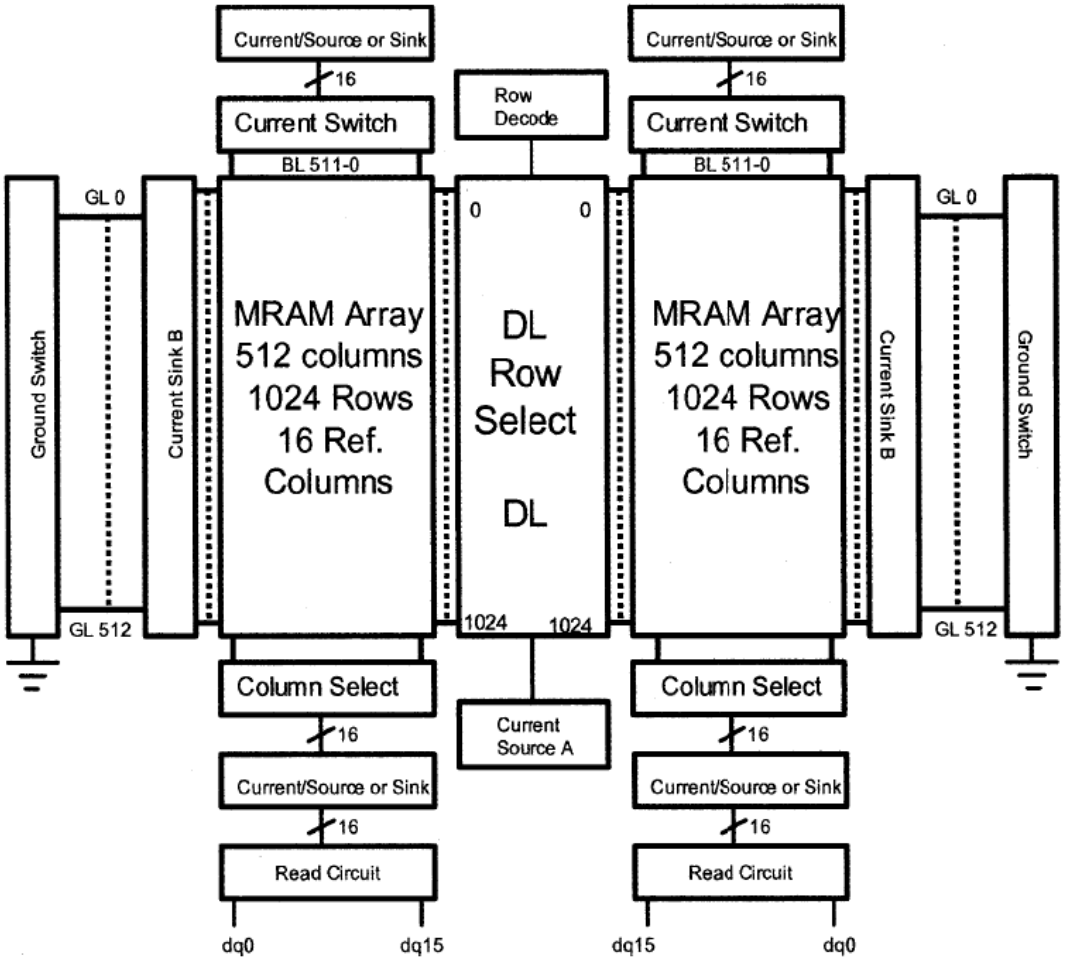


Fig. 9. Block diagram of 1-Mb MRAM.

Durlam 2003

Other MRAM Architectures

- Toggle-MRAM
  - Requires additional circuitry to generate timing signals for the write sequence.
  - Writing a bit first involves reading the bit, then doing a conditional write.
  - Not susceptible to the half-select problem.
- STT-MRAM
  - Promises better power scaling with process dimensions.

Memory Technologies

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Tech.	**Energy**	**Area**	**Speed**	**Memory**	**Config.**	**Flip-Flop**
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Toggle			Less than 25 ns (1)	Commercial		
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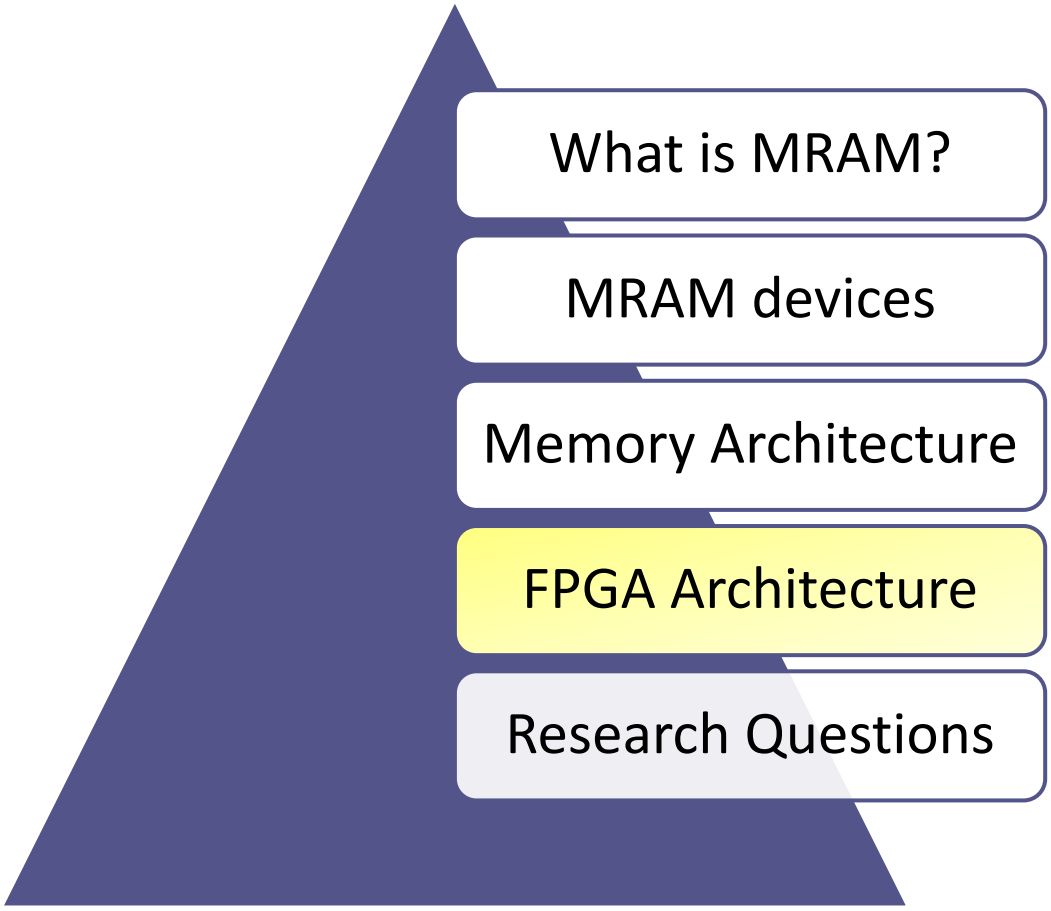
Outline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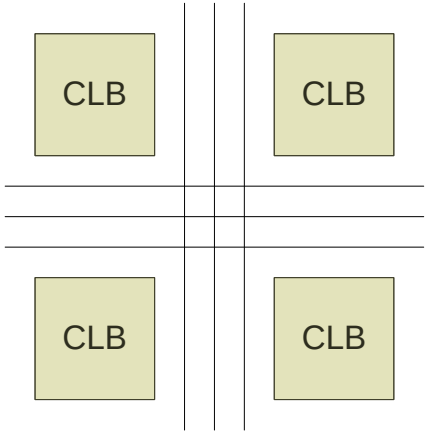
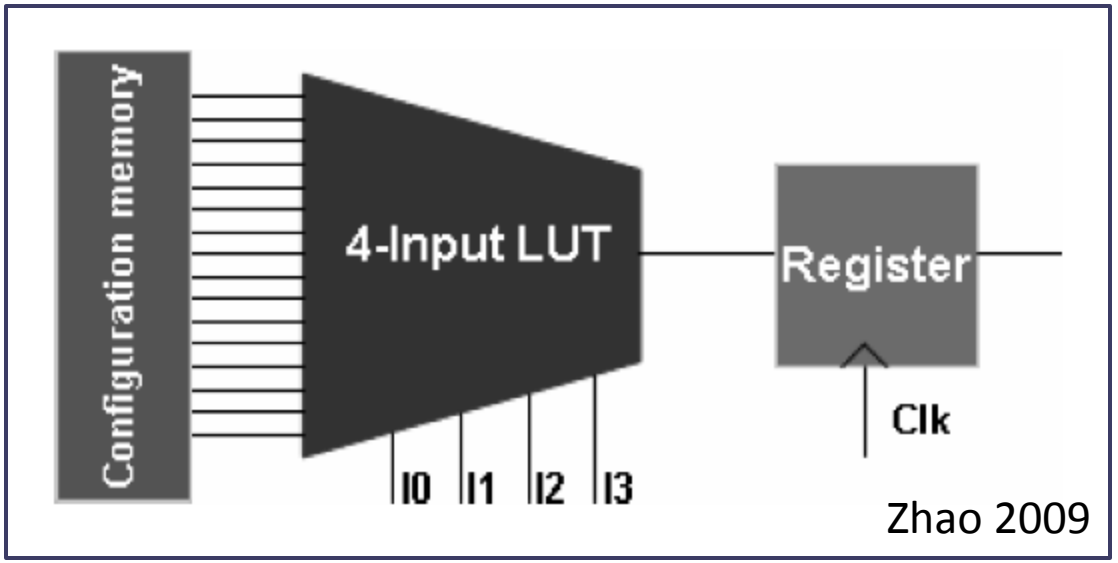
FPGA Architecture

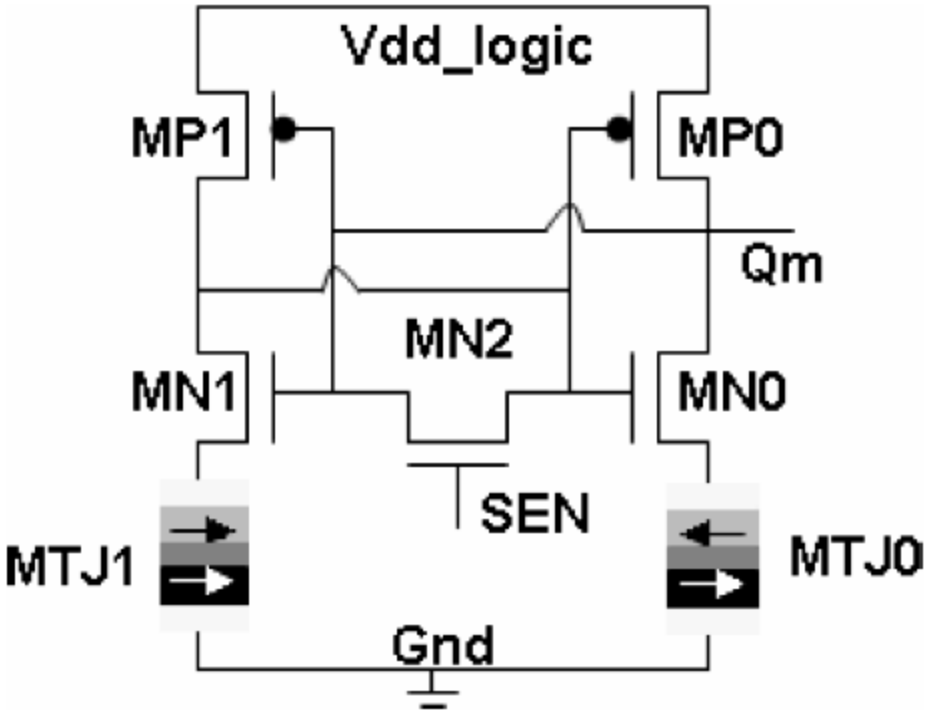


Basic CLB



- Typical FPGA architecture consists of an array of CLBs with routing interconnects.
- A basic CLB contains a LUT and FF.
- Zhao proposes a TAS-MRAM-based LUT and FF that offers nonvolatility, and data security.

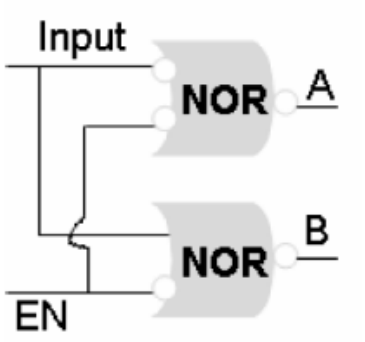
TAS-MTJ Read Circuit

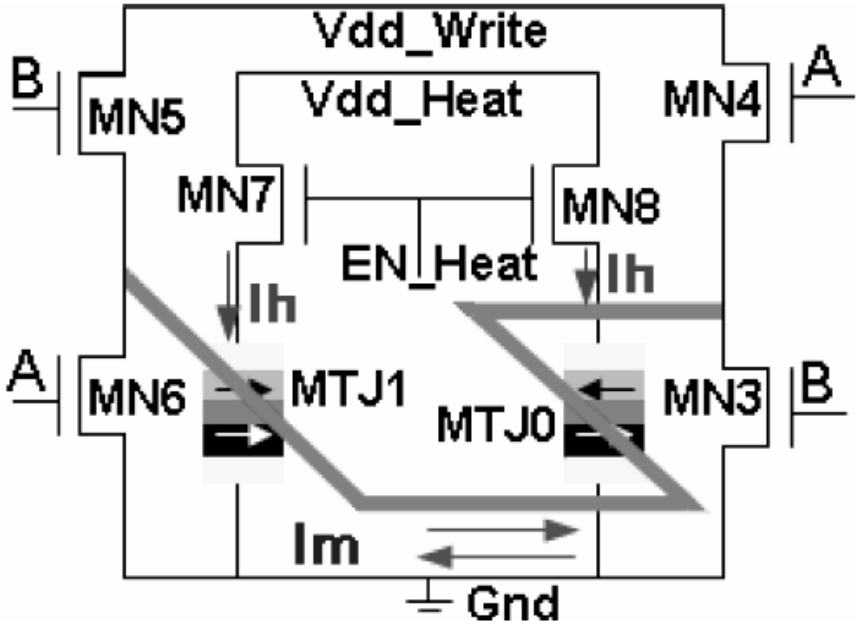


- SRAM-based sense amplifier
- Magnetic orientation of MTJ couple are set opposite to each other
- SEN input senses the state of the MTJs

Zhao 2009

TAS-MTJ Write Circuit





- Two current sources involved in write operation:
  - **Heat current** – raises the temperature of the MTJ above the blocking temperature of the AF layer
  - **I_m current** – bidirectional current used to generate a low intensity magnetic field that switches the free layer of the device

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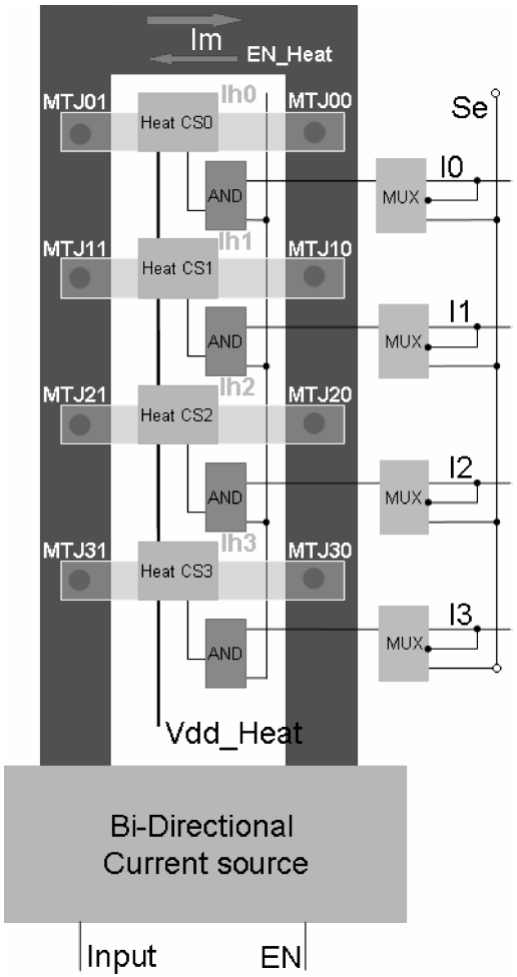
TAS-MRAM-based 2-input LUT



- Four bits of configuration memory
- Each bit has two MTJs, a heat current, and an SRAM-based sense amplifier
- One global bidirectional current source is shared by all bits for the I_m current
- Programming is done in two phases (25 ns total):
  - First the “1” value is programmed
  - Then the “0” value is programmed

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TAS-MRAM-based Nonvolatile Flip-Flop (TAS-FF)

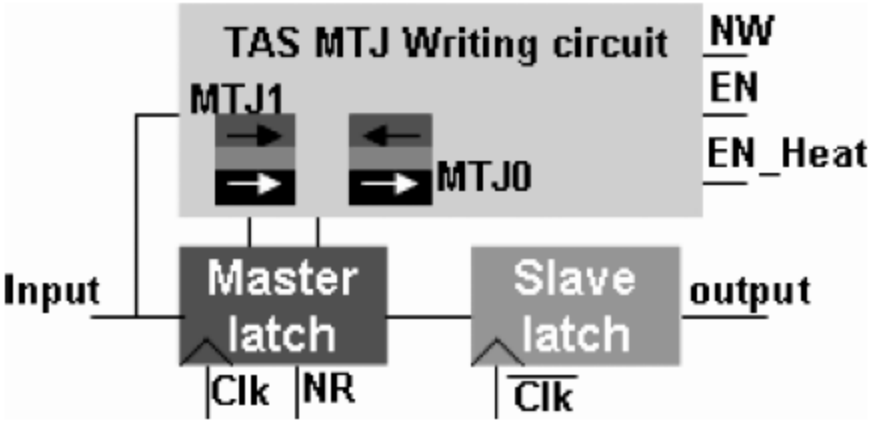

Fig. 19. TAS-MRAM-based nonvolatile flip-flop.

- Uses a conventional D-flip-flop to operate at the normal speed of the FPGA
- Writes data into nonvolatile memory at a lower frequency

Zhao 2009

Compare and Contrast Architectures

MRAM Memory Architectures

- 1 transistor, 1 MTJ cell
- MRAM-based sense amplifier
  - Requires a reference cell and 2 current conveyors
- The memory array is sparsely accessed, so the area consumed by the sense amplifiers is amortized
- Minimize area per cell

FPGA Architectures

- Many transistors, 2 MTJ cells
- SRAM-based sense amplifier
  - 5 transistors
- Every nonvolatile bit accessed in parallel
- Minimize total area

Memory Technologies

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Tech.	**Energy**	**Area**	**Speed**	**Memory**	**Config.**	**Flip-Flop**
FIMS	1.2 nJ		Less than 50 ns (1)	Prototyped	Yes	High energy
Toggle			Less than 25 ns (1)	Commercial	?	?
TAS	0.124 nJ		25 ns prog. latncy.	?	Proposed	Slow
STT	Read 0.155 nJ Write 2.942 nJ	37 F^2	Read 4.7 ns Write 12.3 ns	Promising	Work in progress	Work in progress
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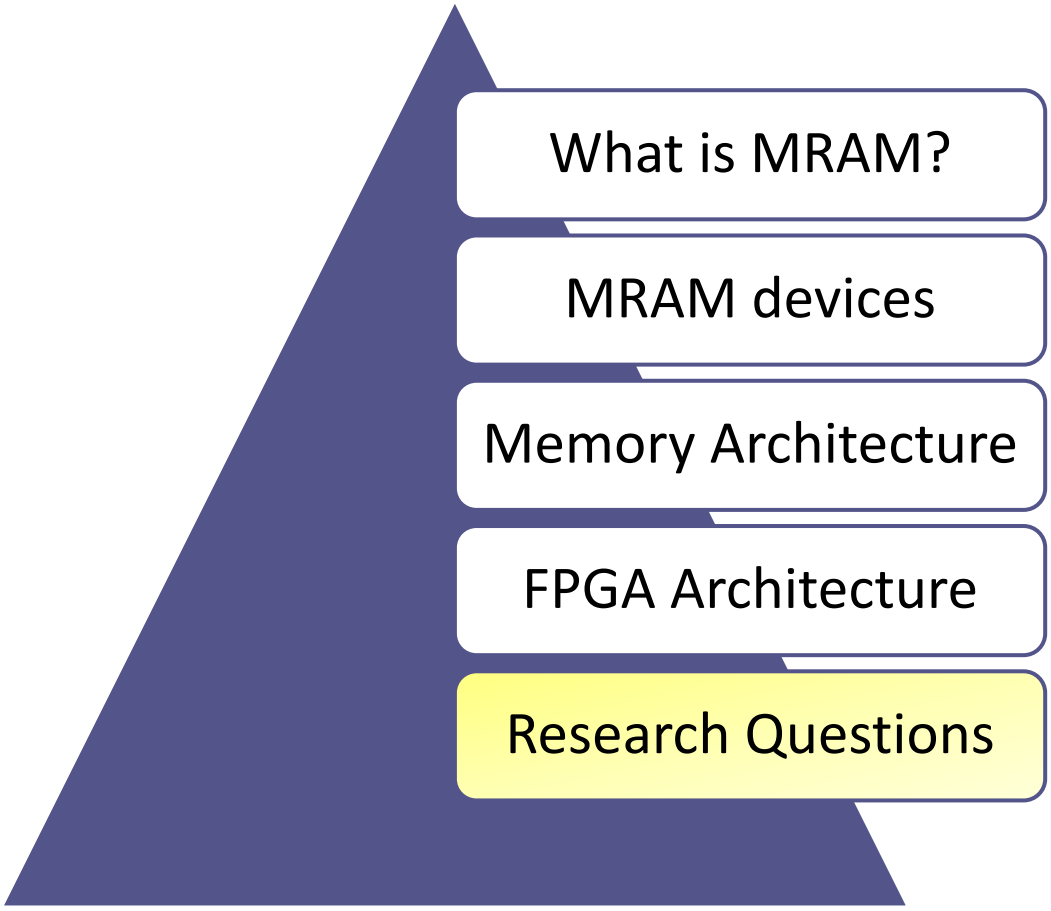
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Research Questions

Research Questions

- Is there a benefit using Toggle-MRAM in FPGAs?
- Is there a benefit using TAS-MRAM in memory arrays? Could the write speed be improved through buffering?
- What is the cause of long cool-down periods for TAS-MRAM? Can this be improved?
- Can simpler sense amp be designed using fewer transistors?
- Can a hybrid chip using TAS-MRAM for configuration memory and STT-MRAM for flip-flops be developed?

Conclusion

- Presented 3 papers in the area of magnetic random access memory (MRAM)
- Discussed the pros and cons of 4 types of MRAM devices
- Presented and compared MRAM memory and FPGA architectures
- Identified several potential areas for new or continued research

References

- Durlam, M. "A 1-Mbit MRAM based on 1T1MTJ bit cell integrated with copper interconnects." IEEE Journal of Solid-State Circuits. May 2003.
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Backup Slides

Key Considerations in MRAM Development

- Tunneling resistance has an exponential relationship to the barrier thickness
- Resistance should be significantly larger than the series resistance of the isolation transistor
  - Necessary to maintain good uniformity of the resistance and magnetoresistance (MR) across the wafer area
- Criterion for feasibility – the distribution of bit-to-bit resistance should have at least 6σ separation from the midpoint of low and high resistance states

Factors Contributing to the Width of the Resistance Distribution

- Variation in bit area – (owing to lithography or etch variations)
- Process damage or veils created during the etch process
- Quality of the MTJ material itself
  - Certain imperfections in the MTJ layers produce tunneling “hot spots” that can carry a significant fraction of the current flowing through a small bit
  - These hot spots could be caused by small variations in thickness
  - Smoother barriers exhibit smaller hot spots in larger numbers
  - The use of amorphous and nanocrystalline materials in the layers beneath the tunnel barrier is critical for controlling this type of roughness.

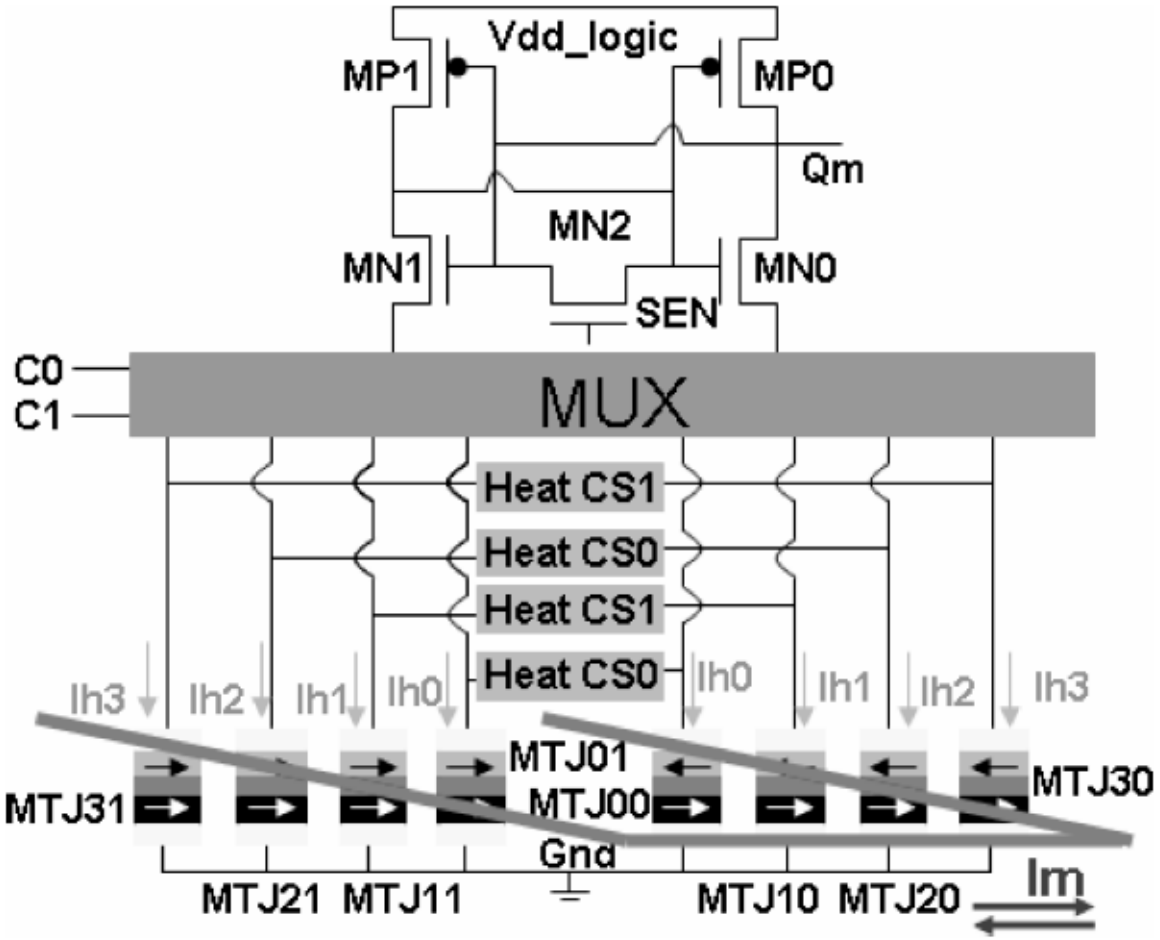
MTJ barrier failure modes

- Two failure modes:
  - **Time-dependent dielectric breakdown (TDDB)** – detected as an abrupt increase of junction current owing to a short forming through a tunnel barrier
  - **Resistance drift** – a gradual reduction of the junction resistance over time that can eventually lead to reduced read margin and, therefore, increased error rate
- Both of these failure modes are accelerated by voltage bias and temperature

Dynamic Reconfiguration

- The SRAM-based sense amplifier will hold its output value until the SEN read input is applied.
- The LUT can be reprogrammed without disturbing the operation of the FPGA.
- The new configuration can be loaded by applying a signal to the SEN read input.

Multi-Context Configuration



- The TAS-LUT can support multiple contexts by modifying each bit:
  - Add a multiplexor to select between contexts (C0, C1).
  - Each context bit has its own heat current source.
  - All context bits share an SRAM-based sense amplifier.
- Writing using the I_m current is still done in 2 phases over all bits in the LUT.

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