Globally Clocked Magnetic Logic Circuits

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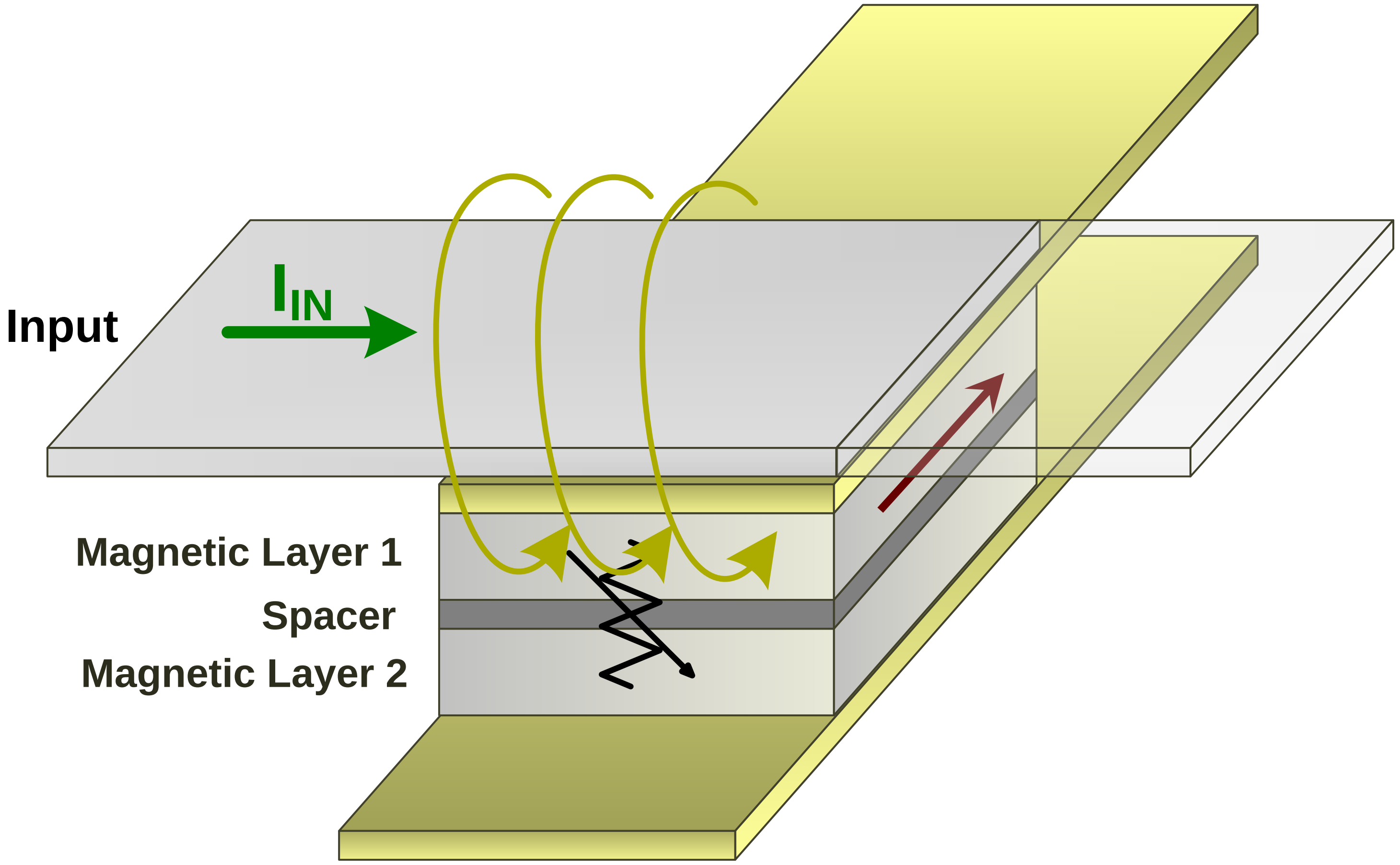
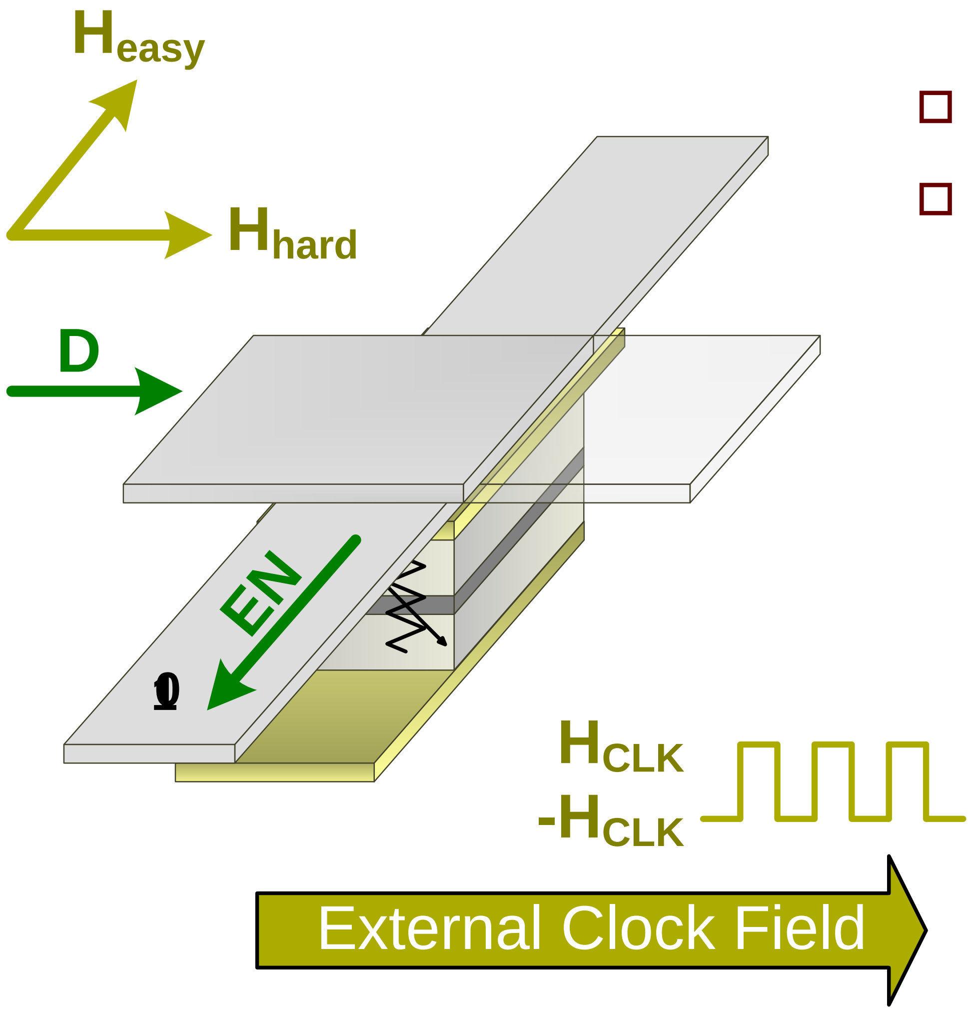
Supported by AFOSR

Spin Valve

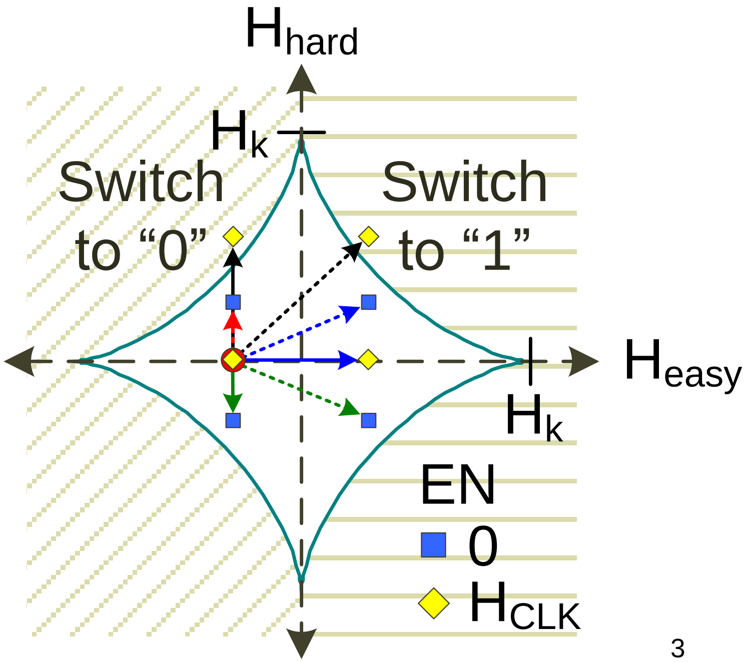


Ney et al. 2003

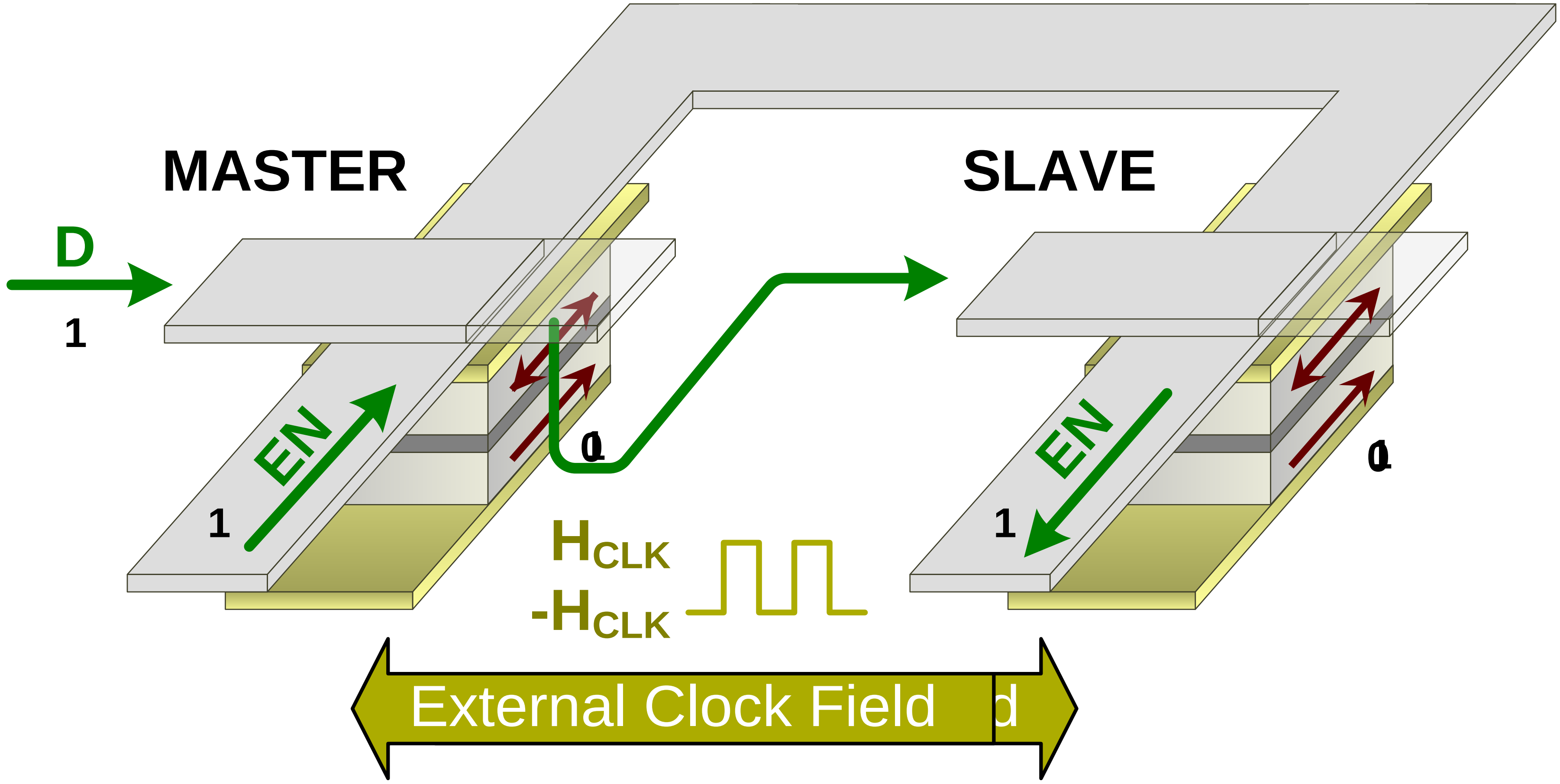
Latch



- Perpendicular current inputs
- Global external clock



Master Slave Flip-Flop



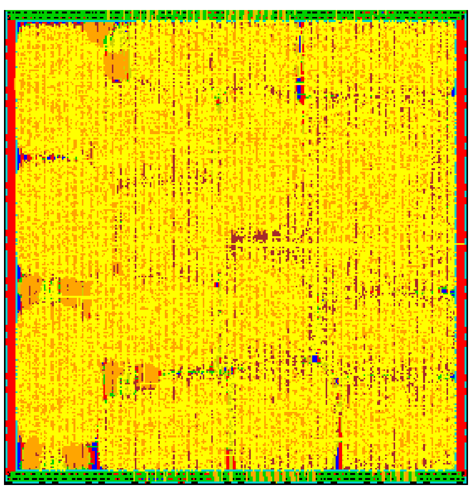
Initial Investigation

- Assessing implications of
  - Replacing all registers with magnetologic memory elements
  - Replacing the clock distribution tree with a global external clock
- Start with standard cell CMOS design
- 2 Applications:
  - Monte Carlo (MC) simulation of π [Singla et al. 2008]
  - Systolic array priority queue (PQ) [Leiserson 1979]

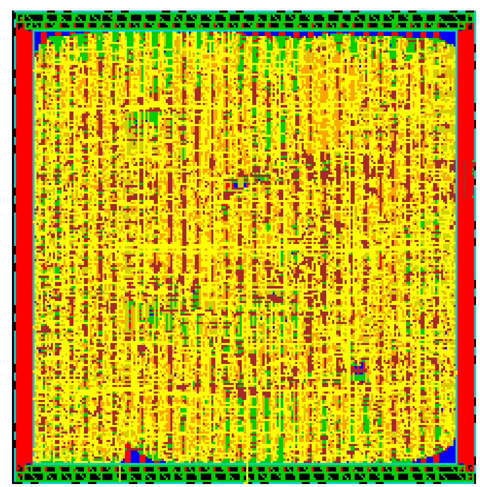
Design Process

- VT 180 nm standard cell design
- HDL → Synthesis → Place & Route
- Estimate power, area, and speed from layout

9.0 mm



MC



4.9 mm

PQ

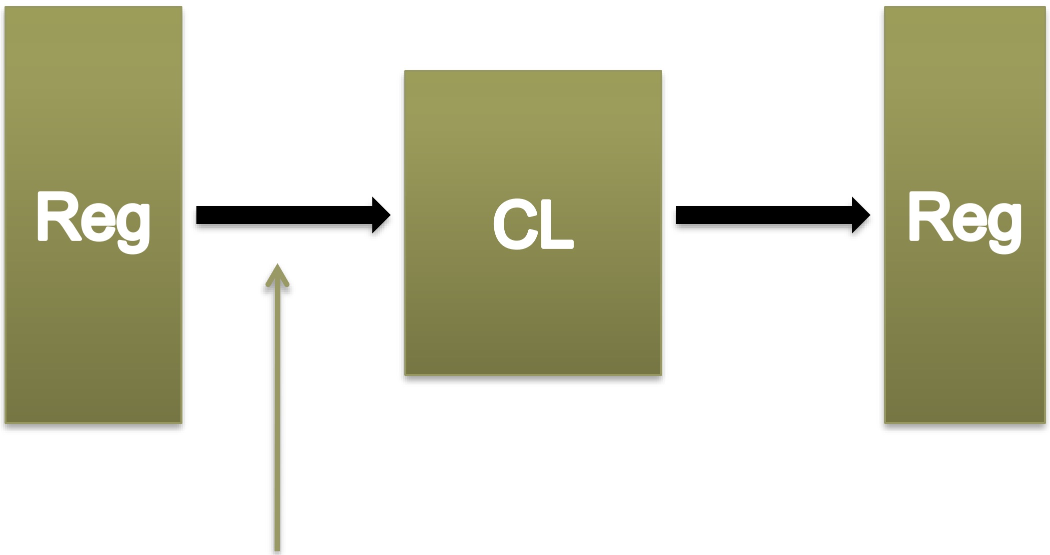
Benchmark Circuit Properties

	MC	PQ
area	75 mm^2	20 mm^2
cell density	86 %	83 %
power	2.7 W	0.8 W
clk freq.	74 MHz	124 MHz
tech.	180 nm	180 nm

Area and Timing Implications

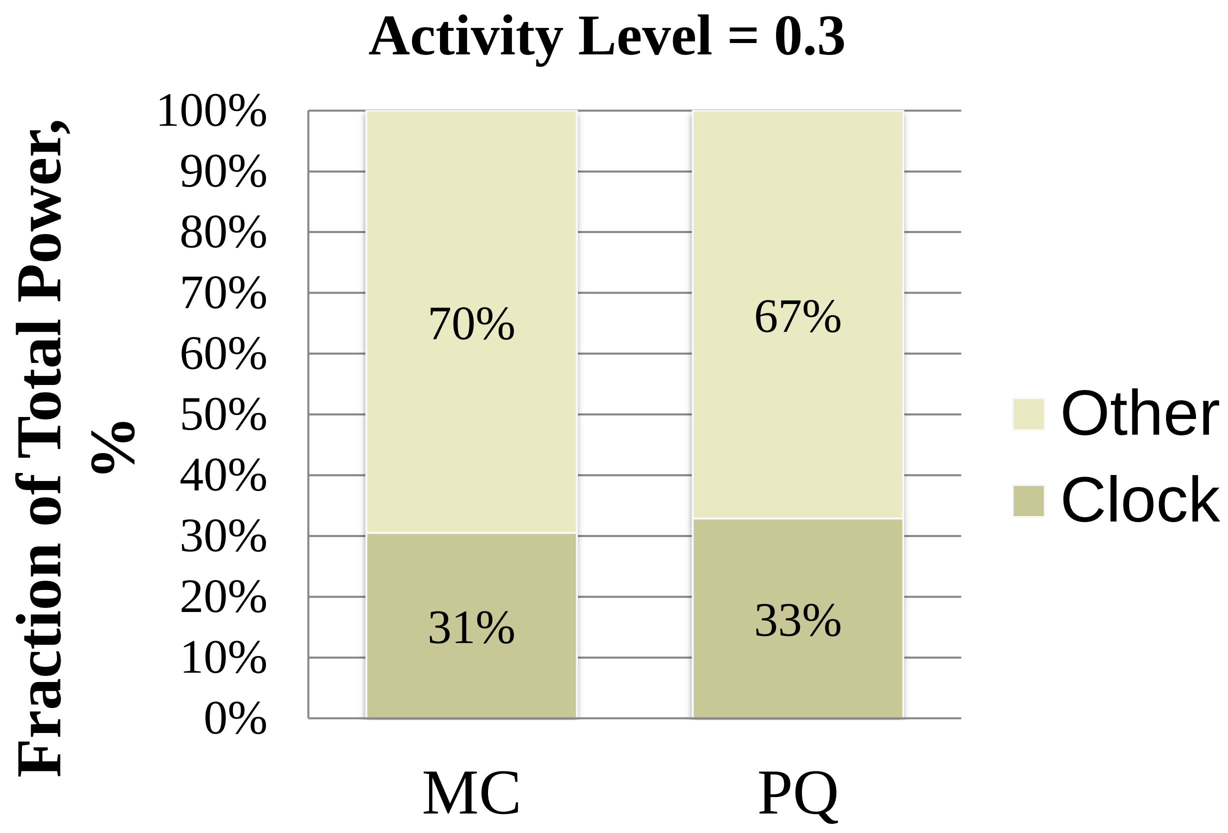
	MC	PQ
clk net area	4 %	8 %
clk skew	342 ps	239 ps
skew %	3 %	3 %

Activity Level



Fraction of signals that change at each clock

Power Implications



Clock power consumption ranges from 25% to 40%

Summary

CMOS Chip	Hybrid Chip
traditional clock distribution tree	global external field
clock routing	eliminated
clock skew	dramatically reduced
clock power	moved off chip

Next Tasks

- Repeat the measurements at 45 nm
- Design and fabricate a prototype
- Investigate logic elements in the presence of an external field

Conclusion

- Global clocking via an external magnetic field is an interesting approach to large-scale synchronous system design
- Illustrated an enabled latch and its associated master-slave flip-flop
- Potential benefits are significant
  - 4 to 8 % area savings
  - ~ 200 to 400 ps clock skew elimination
  - 25 to 40 % power savings

Questions?