Noise Analysis of a Current-Mode Read Circuit for Sensing Magnetic Tunnel Junction Resistance

Michael J. Hall, Viktor Gruev, and Roger Chamberlain

Washington University in St. Louis

Oregon State University

Supported by AFOSR
FA9550-08-1-0473

May 17, 2011

What are Magnetic Tunnel Junctions (MTJs)?

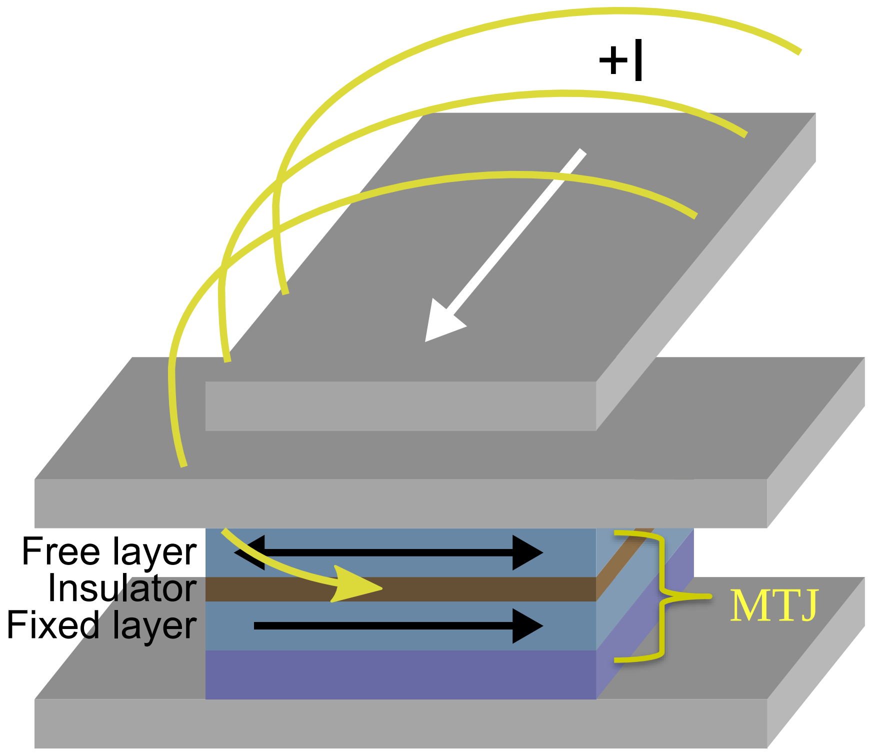
- Small thin-film magnetic devices that are capable of storing information in a magnetic field.

- This information may be accessed by reading the resistance seen through the MTJ device.

- Characteristics:
  - Non-volatile
  - No static power dissipation
  - High write endurance (> 10^{15})

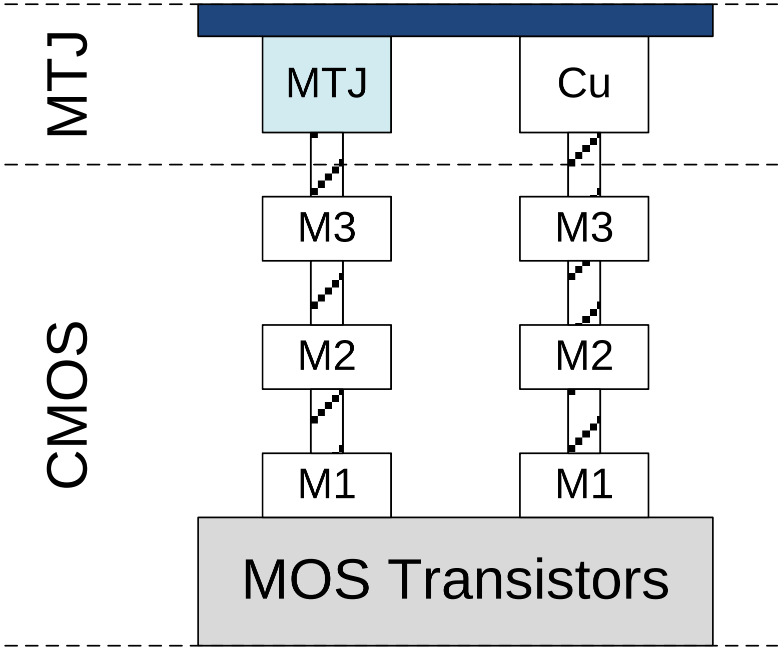
Magnetic device

- Constructed using a magnetic tunnel junction (MTJ) which essentially consists of:
  - Ferromagnetic “free” layer
  - Thin insulator such as MgO
  - Ferromagnetic “fixed” layer
- The device is “set” using a magnetic field generated by a current.
- The device output is a resistance determined by the alignment of the ferromagnetic layers to each other.

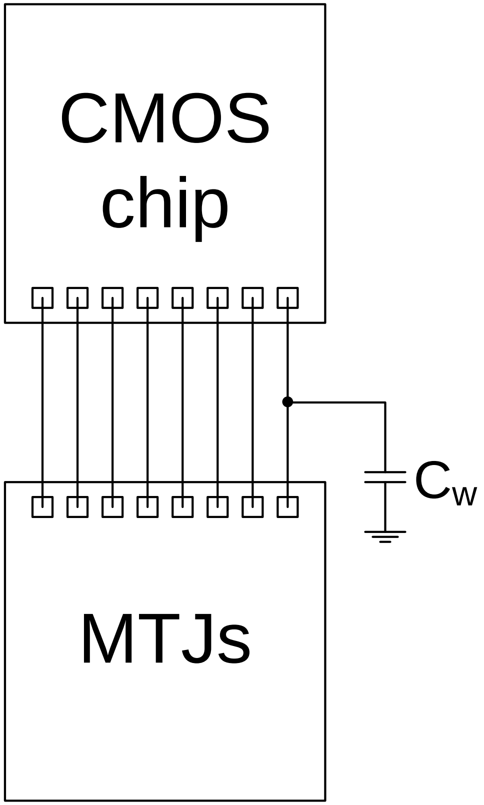


Used in hybrid CMOS-MTJ systems

Integrated



Wirebonded

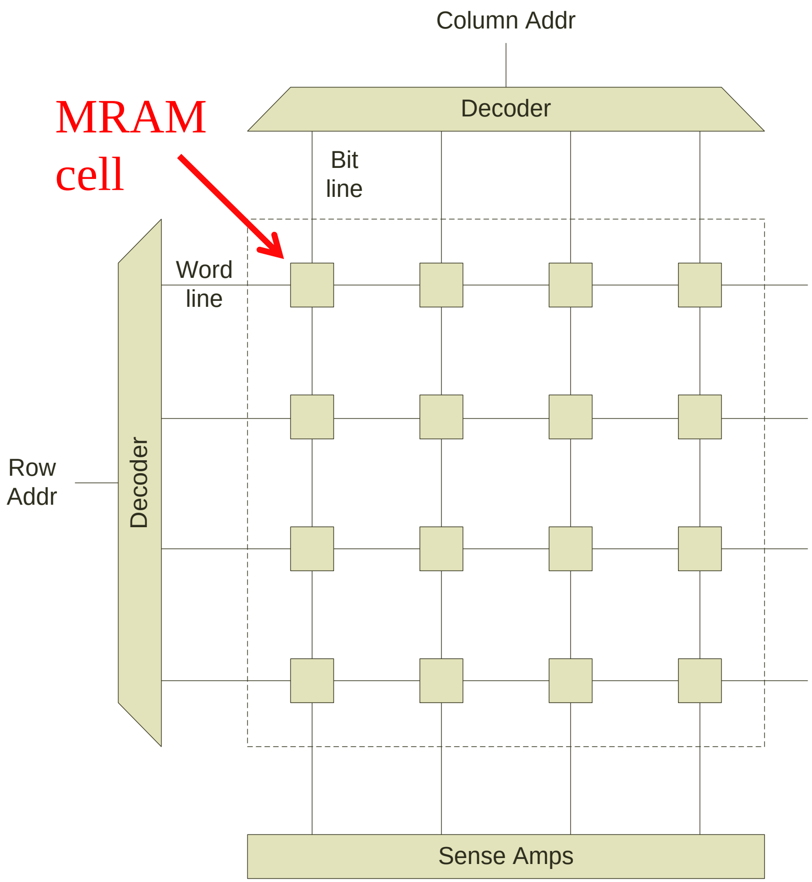


Motivation

- CMOS read circuits are needed to be able to read the resistance state of the MTJ device.

- Example systems include:
  - Memory
  - Computation circuits
  - Global clocking

Memory (MRAM)

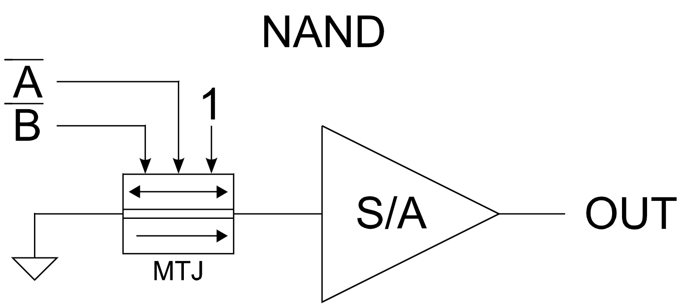


- MRAM cell selected by activating the word line and bit line.
- Sense amp reads MRAM cell, typically using current conveyor circuits.
- Durlam et al., IEEE JSSC 2003

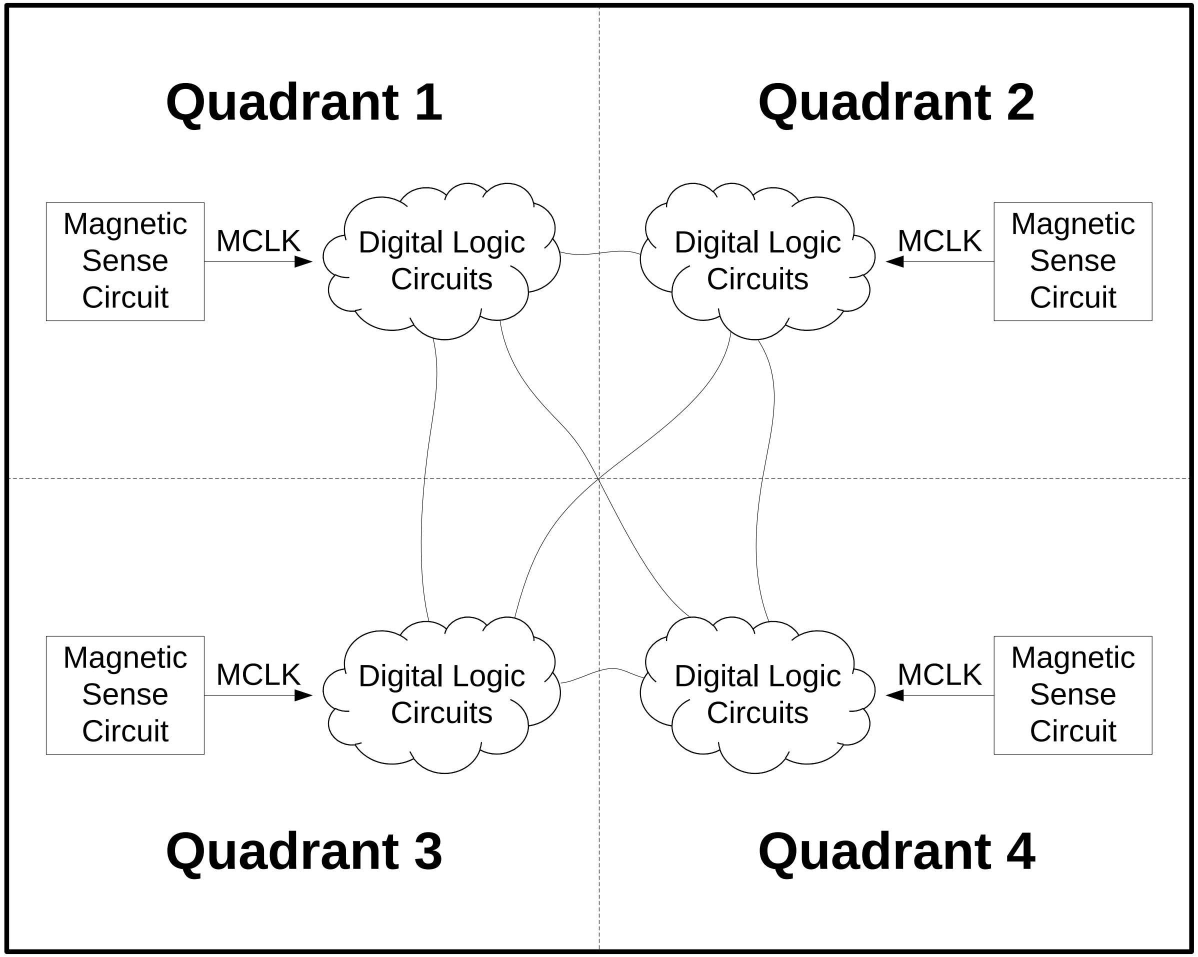
Computation circuits with MTJs

- Digital logic circuits constructed using magnetic devices

Lee et al., IEEE TED 2007



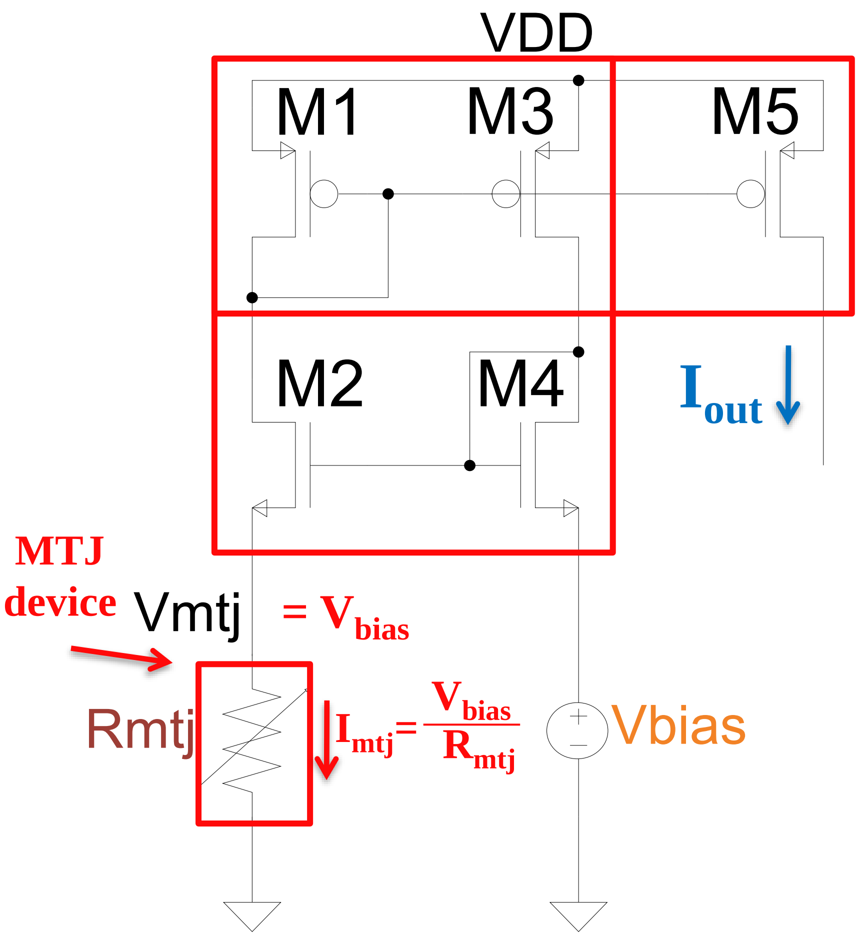
Global clocking using MTJs as magnetic sensors



Our work

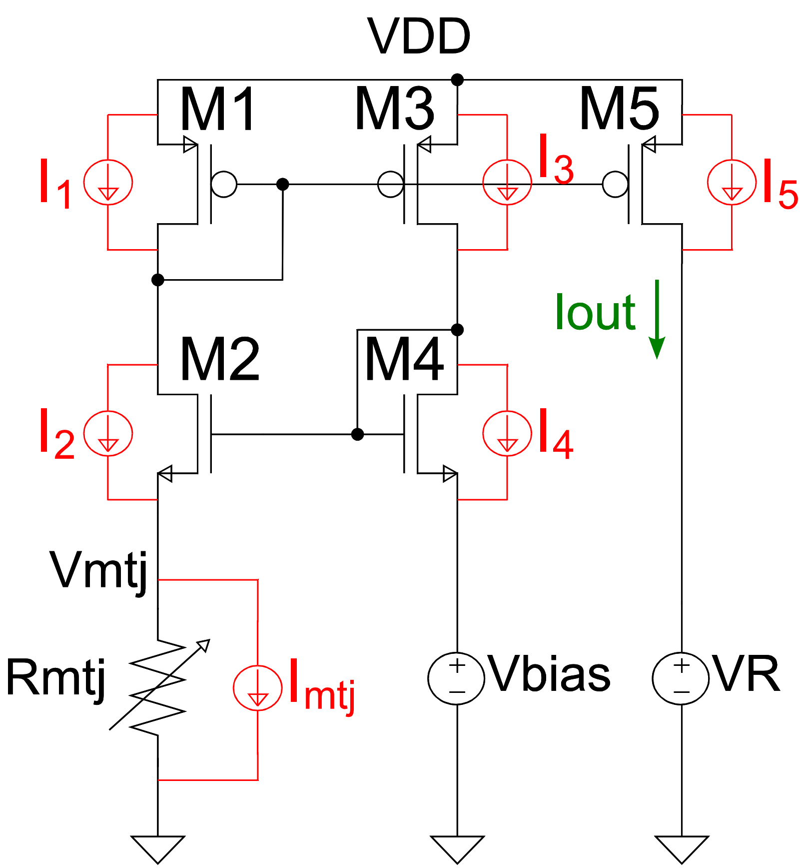
- We chose to design a read circuit using a current-conveyor.
- We subsequently did a noise analysis to understand the effect of noise on the output current.
- We verified our noise equations via simulation.

Current-conveyor read circuit



- Input:
  - MTJ device resistance (denoted by Rmtj)
- Output:
  - I_{out} = Vbias/Rmtj
- Smith and Sedra, Proc of IEEE 1968.

Noise analysis of current-conveyor read circuit



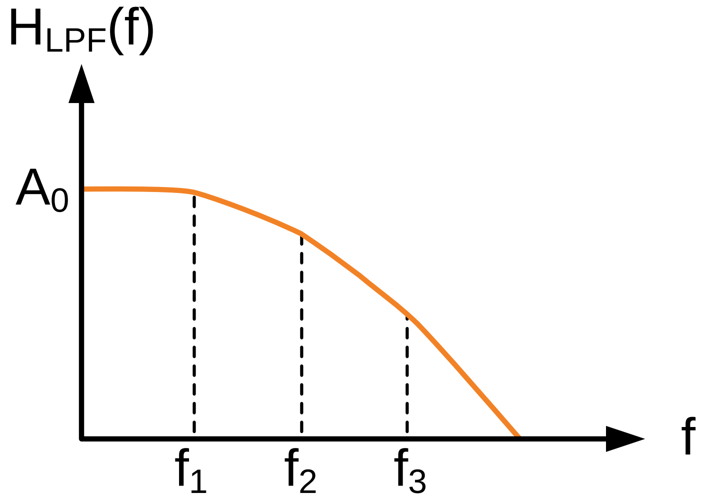
- Noise sources are modeled for every transistor and MTJ device as a current source.
- Small-signal analysis is used to calculate the current gain from noise source-to-output.
- Output referred noise is determined by integrating the noise spectrum across all frequencies.

Noise analysis approach

1. Analytically derive the small-signal DC current gain equations for each noise source, making approximations as allowed to get a simplified form.

2. Determine the pole frequency of each node.

3. Model the noise using a low-pass filter with the bandwidth determined by a 3-pole system.



Noise analysis approach

4. Integrate under the noise power spectrum and take the square root to get the noise current.

Integrated noise power for each source:

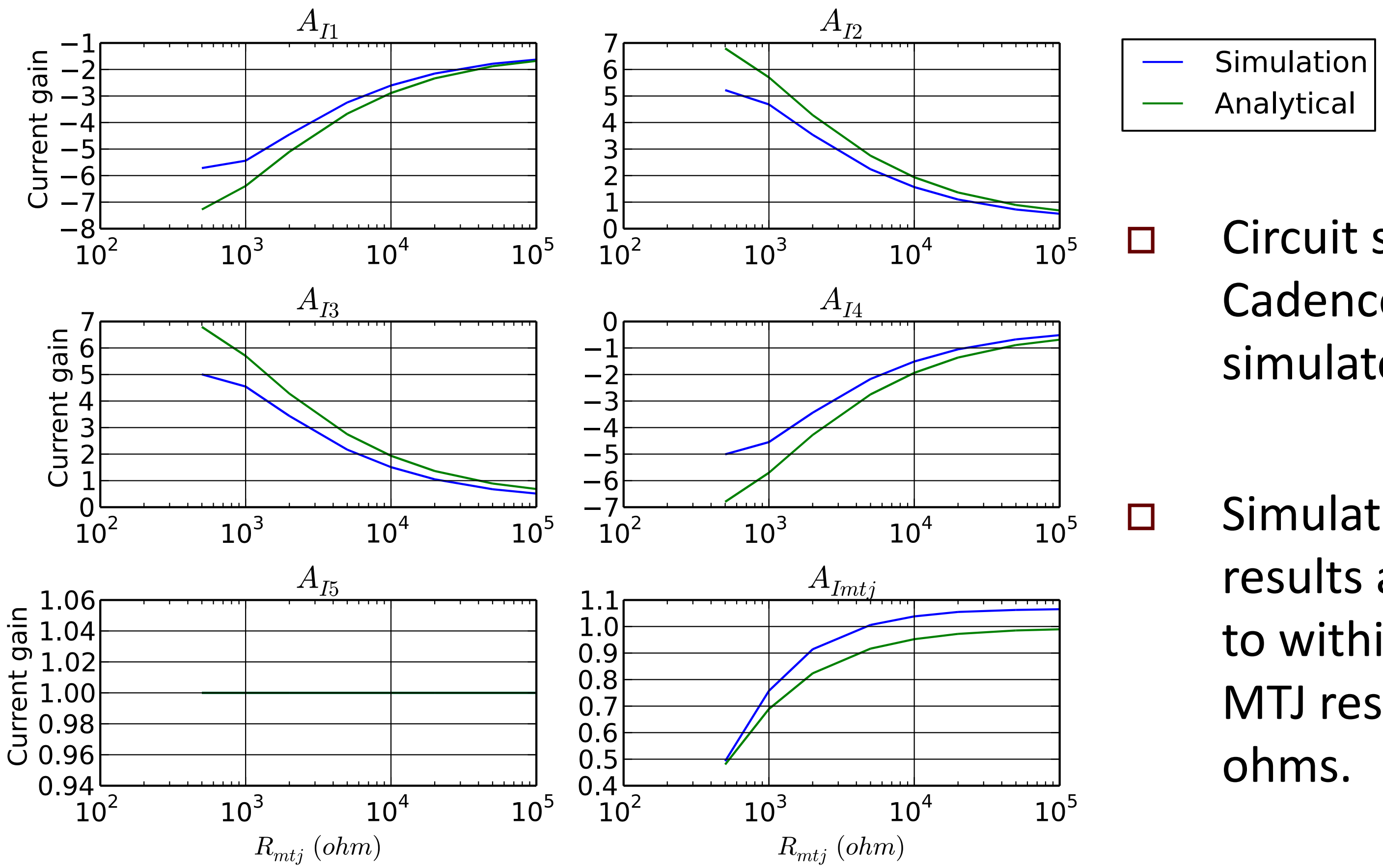
$$\overline{I_n^2} = \int_{f=0}^{f=\infty} S(f)\, df \quad [A^2] \qquad \sigma_n = \sqrt{\overline{I_n^2}} \quad [A]$$

5. Calculate the total noise of all sources by adding all uncorrelated noise contributions in quadrature (sum of the powers).

Superposition of noise powers for k sources:

$$\overline{I_{n,tot}^2} = \overline{I_{n,1}^2} + \overline{I_{n,2}^2} + \ldots + \overline{I_{n,k}^2}$$

Small-signal DC current gain validation

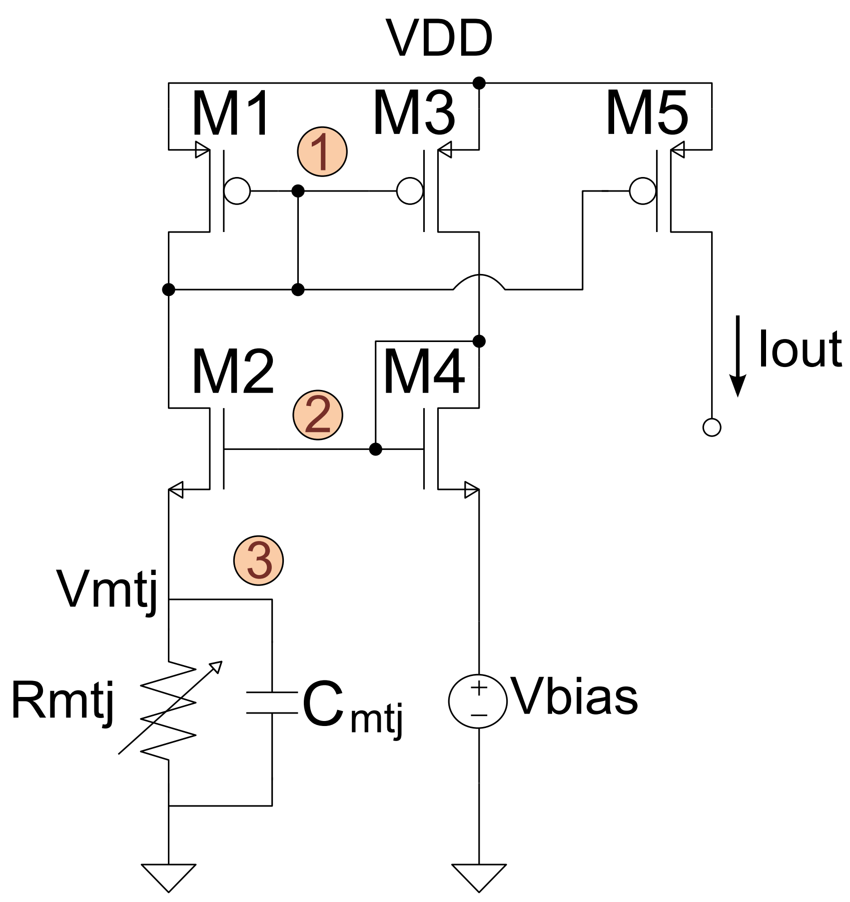


- Circuit simulated in Cadence using Spectre simulator in AMI 0.5u C5N.
- Simulation and analytical results are shown to agree to within about 3 dB at an MTJ resistance of 500 ohms.

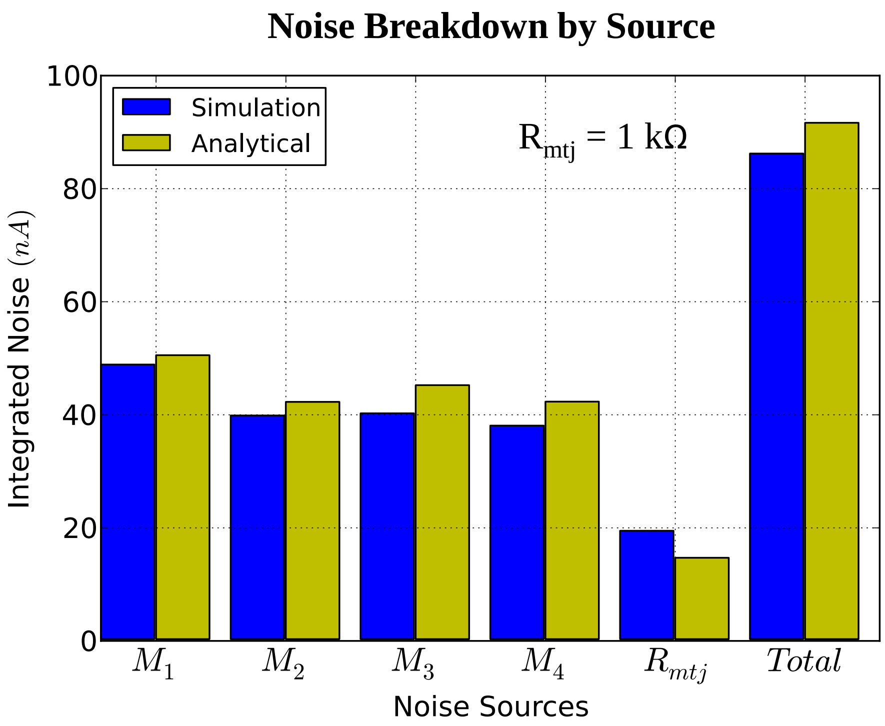
Analytical calculation of pole frequencies

Node	R	C	f_p
1	45.9 kΩ	136 fF	25.5 MHz
2	51.8 kΩ	48 fF	63.9 MHz
3	311 Ω	3.28 pF	156.0 MHz

- 3-pole system
- Assumed C_{mtj} = 3pF
- Input node (node 3)
  - relatively insensitive to the node capacitance
  - has the largest pole frequency



Total integrated output noise validation



- Small signal parameters for the analytical equations were obtained from the DC operating points in the circuit simulation.
- Simulation and analytical results are within 2.5 dB for each noise source.

Noise margins

- Tolerance to distinguish between logic 0 and 1.
- For R_H=1,000Ω, R_L=500Ω, V_{BIAS}=0.1V, σ=91nA
  - I_L=100µA, I_H=200µA
- $I_H - I_L >> 10\sigma$
- Internal thermal noise is insignificant for establishing a noise margin.

Future work

- Expand this noise analysis to cascoded current conveyors.
- Further investigation of noise margins. For example:
  - Process variations
  - External noise sources
  - Power supply

Conclusions

- Derived a set of output noise equations for the current-conveyor read circuit.
- Verified equations against simulated results.
- Observed that the circuit bandwidth is relatively insensitive to the input capacitance.
- Internal thermal noise is insignificant for establishing noise margins for digital circuits.

Questions?